Double-Data-Rate QPI PSRAM

Specifications

- Single Supply Voltage:
  - V_{DD} =1.62 to 1.98V
- Interface: QPI (quad peripheral interface)
- Performance: Clock rate up to 166MHz
- Organization: 128Mb, 16M x 8bits
- Addressable Bit Range: A[23:0]
  (array accesses must start on EVEN addresses only, e.g., A[0]=0)
- Page Size: 2048 bytes
- Refresh: Self-managed
- Operating temperature range
  - T_{OPER} = -40°C to +85°C (standard range)*
  - T_{OPER}= -40°C to +105°C (extended range)*
- Maximum Standby Current:
  - 590µA @ 105°C
  - 420µA @ 85°C
- Halfsleep™ Mode with data retained:
  - 19.5µA @ 25°C

Features

- 50, 100 & 200Ω Configurable Output Drive Strength LVCMOS.
- Register configurable wrap lengths of 16,32,64 and 2048.
- Software reset.
- Data mask (DM) for write operation
- Data strobe (DQS) for high speed read operation
- **Ultra Low Power Halfsleep™ Mode** with data retention.

Table of Contents

1 Table of Contents

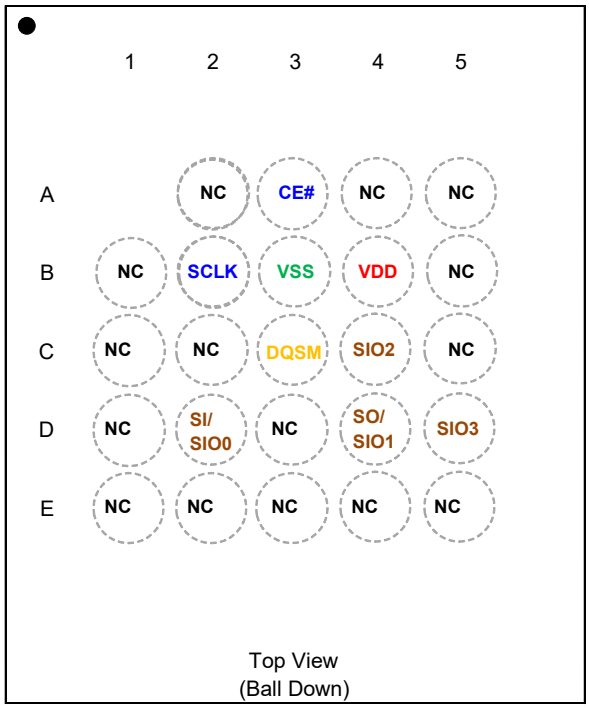
2 Introduction

This Pseudo-SRAM device features a high speed, low pin count interface. It has 4 DDR I/O pins and operates in QPI (quad peripheral interface) mode with frequencies up to 166 MHz. The data input (A/DQ) to the memory relies on clock (CLK) to latch all instructions, addresses and data. It is most suitable for low-power and low cost portable applications. It incorporates a seamless self-managed refresh mechanism. Hence it does not require the support of DRAM refresh from system host. The self-refresh feature is a special design to maximize performance of memory read operation.

3 Package Information

The APS12804O-DQX-BA is available in mini-BGA 24B package 6 x 8 x 1.2mm, ball pitch 1.0mm, ball size 0.4mm package code(BA) .

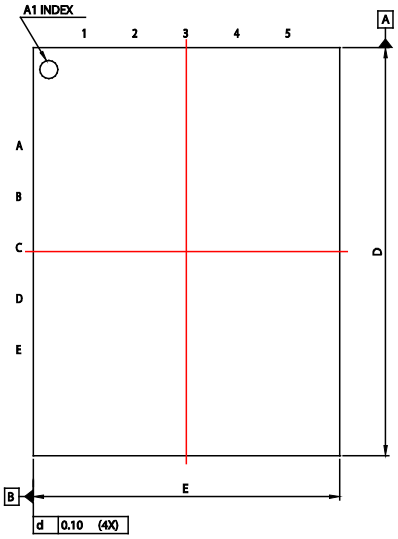
- Ball Assignment for MINI-BGA 24B



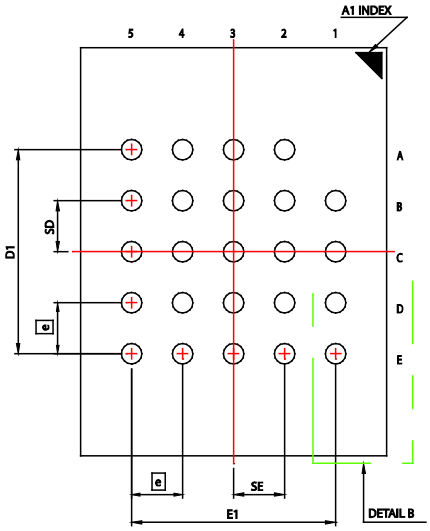
(6x8x1.2mm)(P1.0)(B0.4)

4 Package Outline Drawing

TOP VIEW

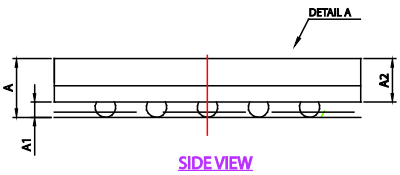


BOTTOM VIEW

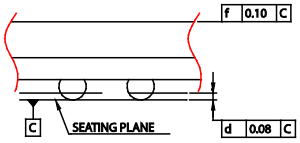


SYM.	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.25	0.30	0.35
A2	-	0.79	-
b	0.35	0.40	0.45
D	7.90	8.00	8.10
D1	4.00 BSC		
E	5.90	6.00	6.10
E1	4.00 BSC		
SE	1.00 TYP		
SD	1.00 TYP		
e	1.00 BSC		

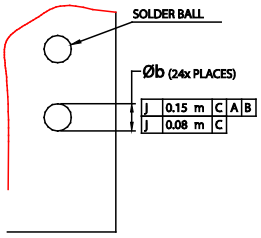
NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.
3. THE DIAMETER OF PRE-REFLOW SOLDER BALL IS Ø0.40mm.(0.35mm SMO)



SIDE VIEW



DETAIL A

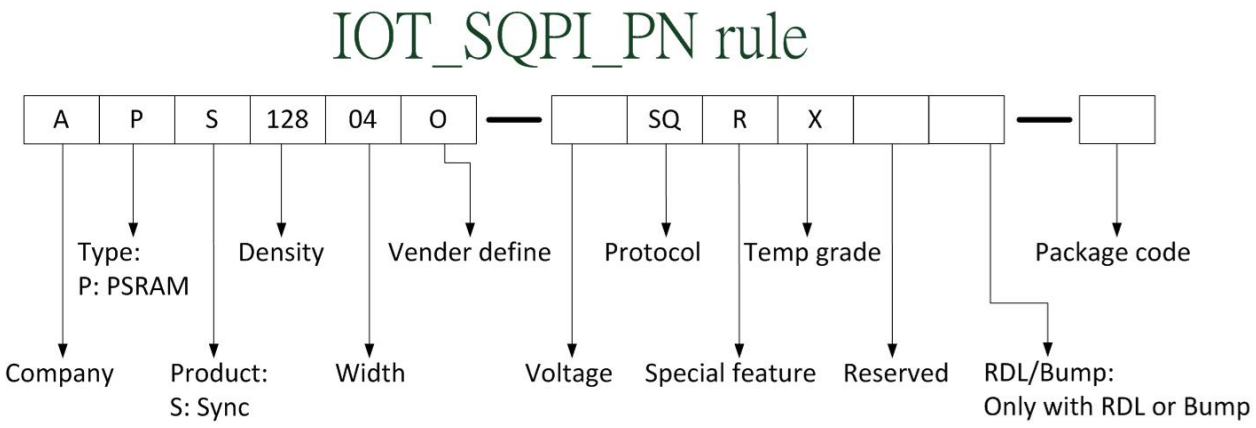


DETAIL B

5 Ordering Information

Table 1: Ordering Information

Part Number	*IO*	*Temperature Range*	*Max Frequency*	*Note*
APS12804O-DQ	X4	T_j=-40°C to +85°C	166 MHz	Bare die, SIP
APS12804O-DQX	X4	T_j=-40°C to +105°C	166 MHz	Bare die, SIP
APS12804O-DQX-BA	X4	Tc=-40°C to +105°C	166 MHz	BGA 24B (only for validation purpose)



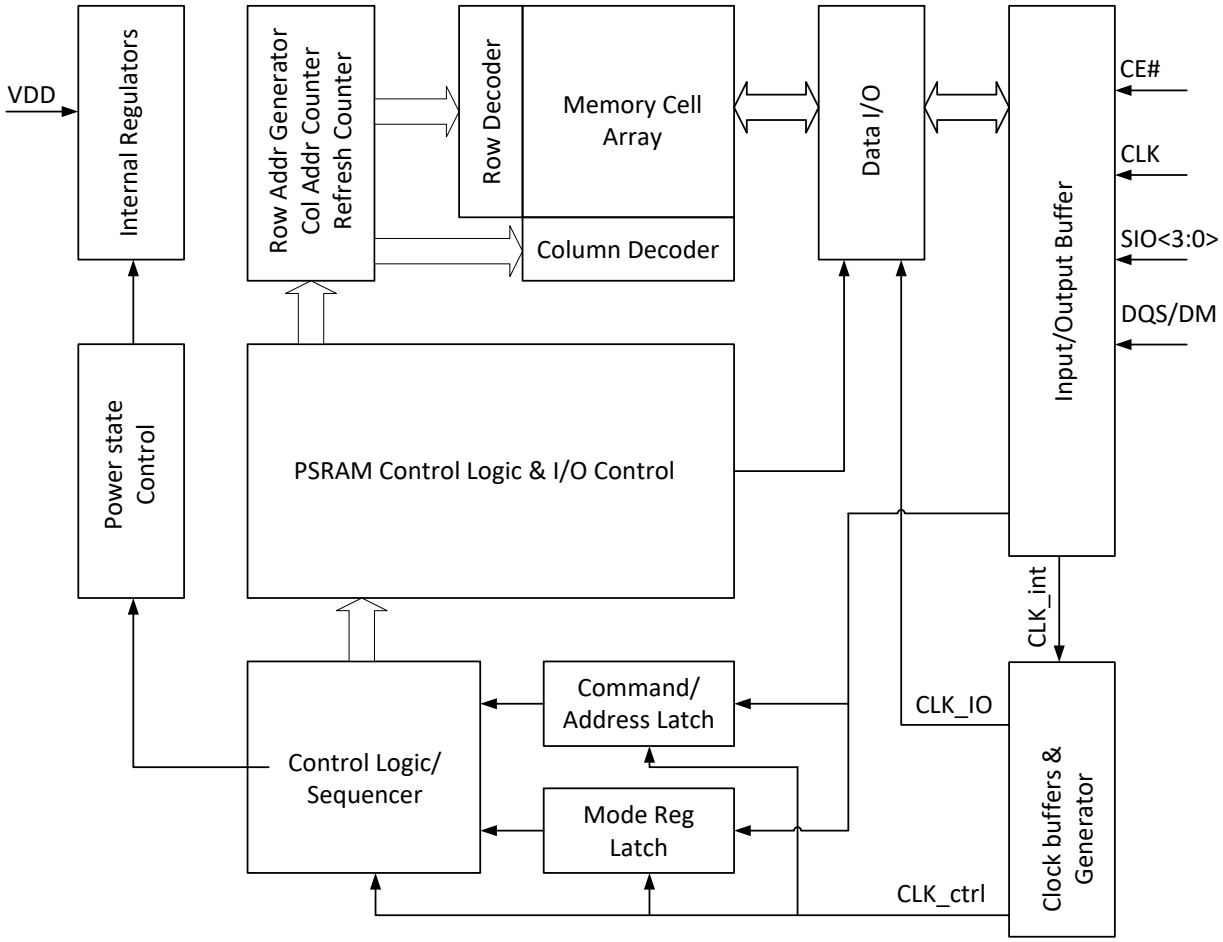
6 Signal Table

All signals are listed in Table 2.

Table 2: Signals Table

Symbol	*Type*	*Description*	*Comments*
V_{DD}	Power	Core & IO supply 1.8V	
V_{SS}	Ground	Core& IO supply ground	
CE#	Input	Chip select, active low, When CE#=1 chip is in standby	
SIO[0]	IO	IO[0]	
SIO[1]	IO	IO[1]	
SIO[2]	IO	IO[2]	
SIO[3]	IO	IO[3]	
DQS/DM	IO	Data mask during memory writes, DQS during memory reads	DM function can be disabled via MR0[7]
CLK	Input	Clock signal	

7 Block Diagram



8 Power-Up Initialization

QPI products include an on-chip voltage sensor used to start the self-initialization process. When V_{DD} reaches a stable level at or above minimum V_{DD}, the device will require 150µs and user-issued RESET Operation to complete its self-initialization. From the beginning of power ramp to the end of the 150µs period, CLK should remain LOW, CE# should remain HIGH (track V_{DD} within 200mV) and SI/SO/SIO[3:0] should remain LOW.

After the Device Reset tRST≧50ns period the device is ready for normal operation.

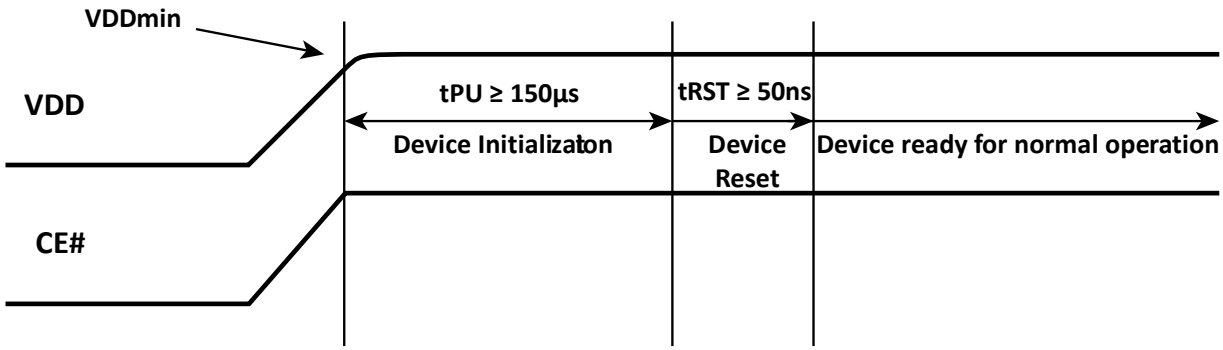


Figure 1. Power-Up Initialization Timing

9 Interface Description

9.1 Address Space

QPI PSRAM device is byte-addressable. 128M device is addressed with A[23:0].

9.2 Page Length

Read and write operations have a page size of 2048 bytes.

9.3 Drive Strength

The device powers up in 50Ω.

9.4 Power-on Status

The device powers up in DDR QPI Mode. It is required to have CE# high before beginning any operations.

10 Mode Register Definition

Table 3: Mode Register Table

MR No.	MA[3:0]	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	`h0	R/W	DM	Wrap		Latency			DQ Zout	

Table 4: Data Mask Config MR0[7]

Data Mask (DM)	
MR0[7]	DM function
0 (default)	ON
1	OFF

Table 5: Wrap Codes MR0[6:5]

Wrap Burst Settings	
MR0[6:5]	Wrapped Length
00	16
01	32
10	64
11 (default)	2048 (page size)

Table 6: Latency Configuration Codes MR0[4:2]

Latency Codes (LC)			*Max Input CLK Freq (MHz)*	
MR0[4:2]	***Write Latency (LC)***	***Read Latency (LC+1)***	***Standard***	***Extended***
010	2	3	84	84
011	3	4	104	104
100 (default)	4	5	133	133
101	5	6	166	166
others	reserved	-	-	-

Table 7: DQ Output Drive Strength Codes MR0[1:0]

DQ Output Drive Strength	
MR0[1:0]	***Impedance***
00 (default)	50Ω
01	100Ω
10	200Ω
others	reserved

11 Command/Address Latching Truth Table

The device recognizes the following commands.

Command	*Code*	*Cmd*	*Addr*	*Wait Cycle*	*DIO*	*Max Freq.*
Wrapped Read	'h8B	Q	Q	LC+1	Q	166
Wrapped Write	'h82	Q	Q	LC	Q	166
Mode Register Read	'hB5	Q	Q	LC+1	Q	166
Mode Register Write	'hB1	Q	Q	0	Q	166
Reset Enable	'h66	Q	-	-	-	166
Reset	'h99	Q	-	-	-	166
Halfsleep™ Entry	'hC0	Q	-	-	-	166

Remark: Q = Quad IO; Command cycles are SDR, Address and Data cycles are DDR, Fmax 166MHz

11.1 Command Termination

All Reads & Writes must be completed by raising CE# high immediately afterwards in order to terminate the active read/write wordline and set the device into standby. Not doing so will block internal refresh operations and cause memory failure. For write operations sufficient ^{t}CHD will ensure final write data is latched and written, while ^{t}CSP2 ensures no extra writes occurs once CE is HIGH.

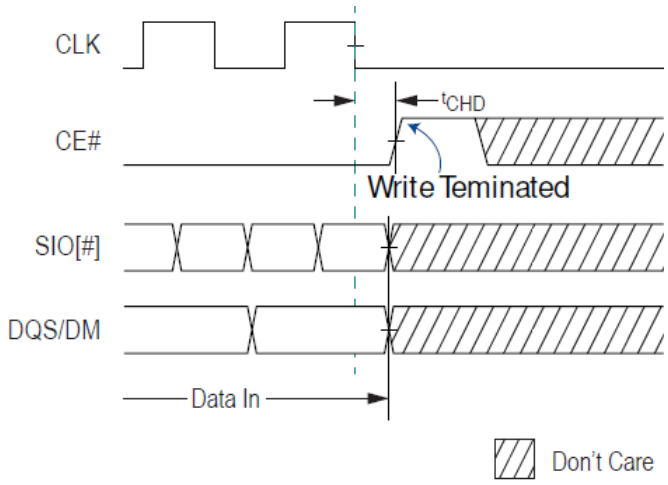


Figure 2: Write Command Termination (no CLK during CE high)

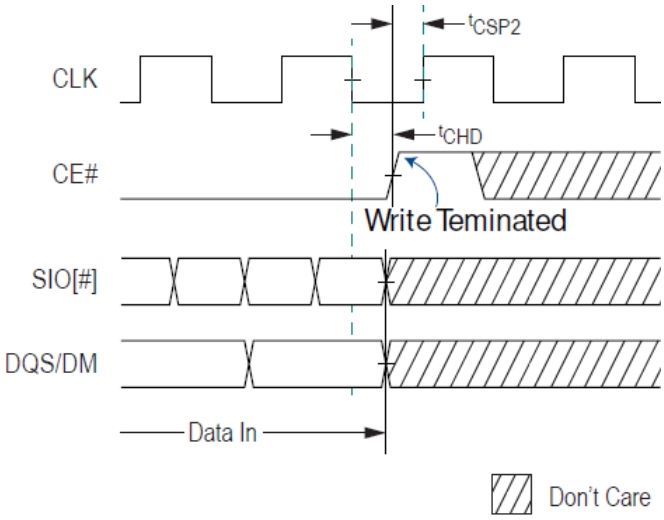


Figure 3: Write Command Termination (CLK during CE high)

For a memory controller to correctly latch the last piece of data prior to read termination, it is recommended to provide a longer CE# hold time (^{t}CHD +^{t}HZ> ^{t}DQSCK) for a sufficient data window.

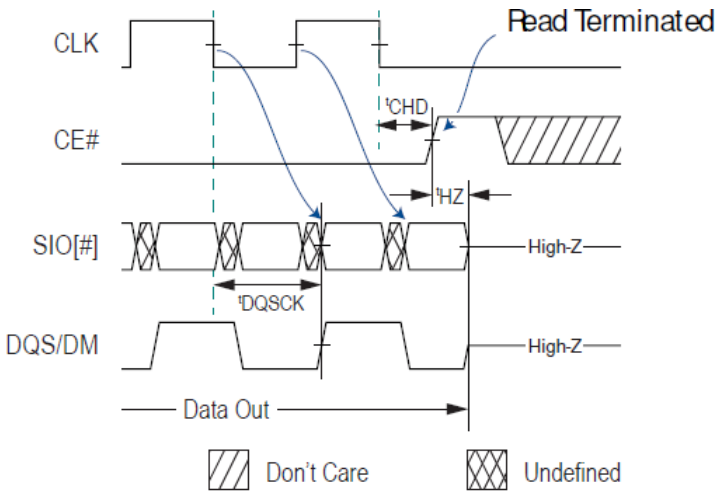


Figure 4: Read Command Termination

12 Halfsleep™ mode Operation

Halfsleep™ Mode is a feature which puts the device in an ultra-low power state, while the stored data is retained. Halfsleep™ Mode Entry can be entered by issuing a command 'hC0. CE# going high initiates the Halfsleep™ mode and must be maintained for the minimum duration of tHS. The Halfsleep™ Entry command sequences are shown below.

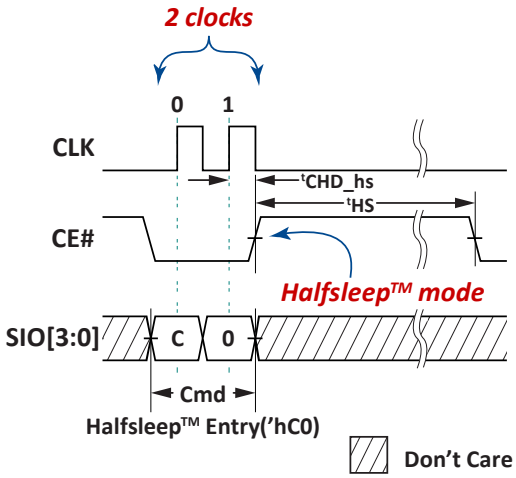


Figure 5: QPI Halfsleep™ Entry 'hC0.

Halfsleep™ Exit is initiated by a low pulsed CE#. Afterwards, CE# can be held high with or without clock toggling until the first operation begins (observing minimum tXHS).

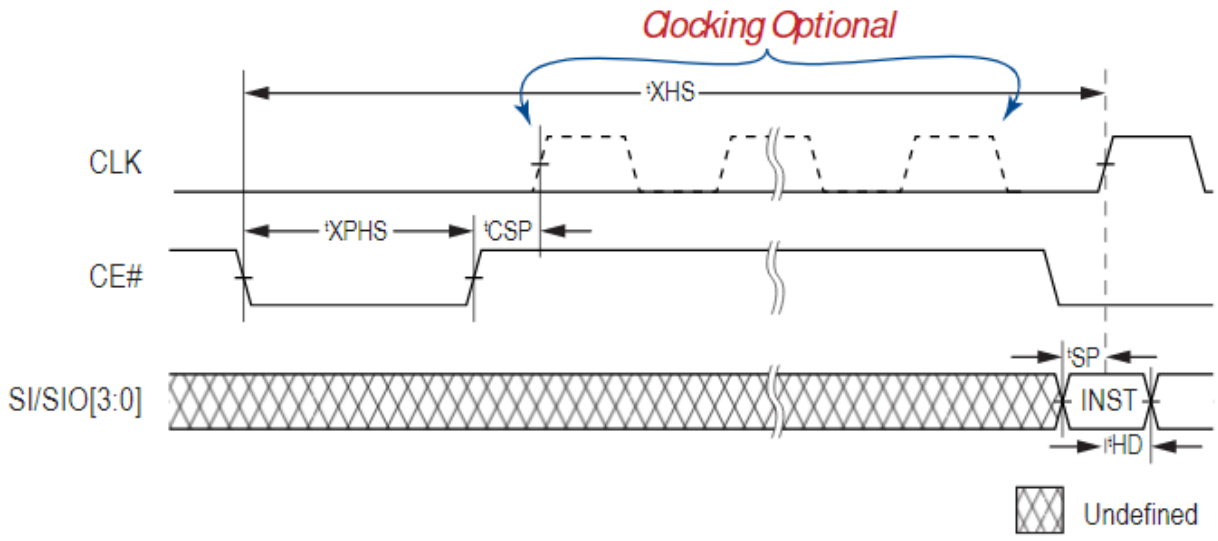


Figure 6: Halfsleep™ Exit

13 Mode Register Operations

13.1 QPI MR Read Operation

For all reads, MR data will be available ^{t}DQSCK after the falling edge of CLK.

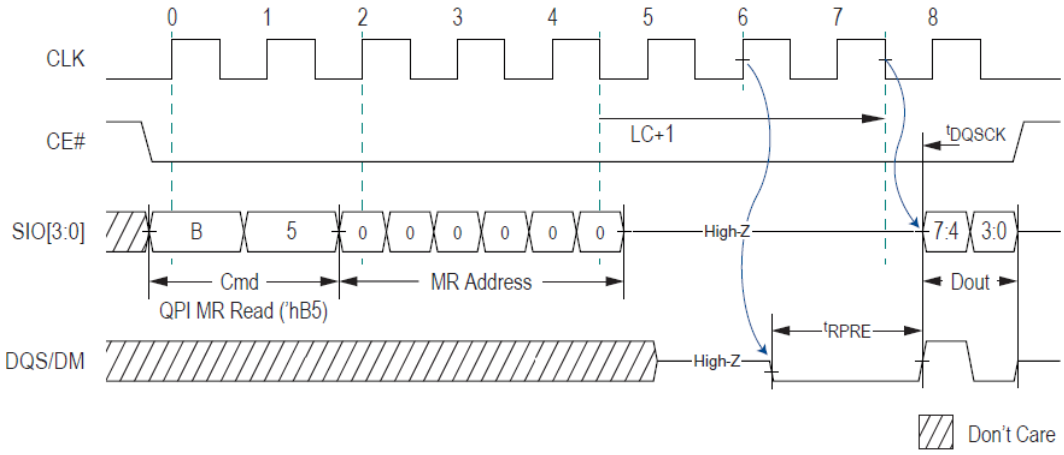


Figure 7: QPI MR Read 'hB5 (Latency Code 2 shown)

13.2 QPI MR Write Operation

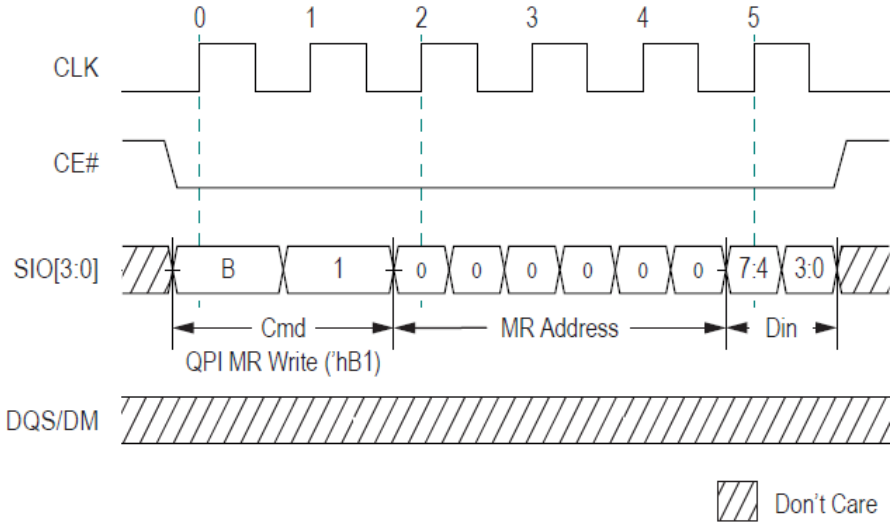


Figure 8: QPI MR Write 'hB1

14 Memory Operations

Write and read operations must start on even addresses (e.g., A[0]=0) only. Minimum read or write length is 1 byte.

Note that for DM disabled devices (MR0[7]=1) the Host will still need to disable their DQS input buffer outside of array read operations since the memory device will only drive DQS pin during array read data cycles.

14.1 QPI Read Operations

For all reads, data will be available ^{t}DQSCK after the falling edge of CLK.

QPI Reads can be done by issuing the command 'h8B.

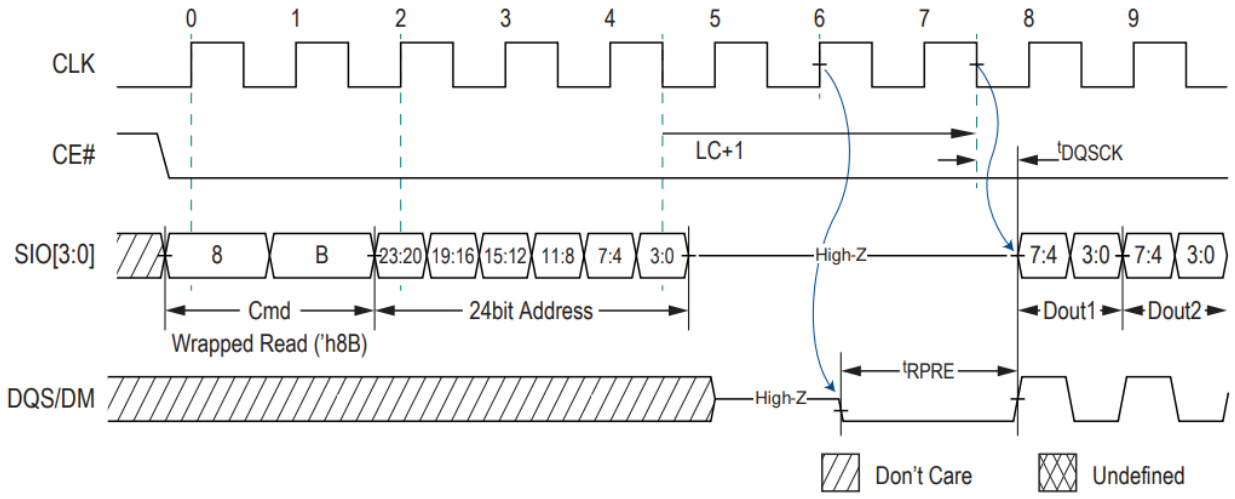


Figure 9: QPI Read 'h8B (Latency Code 2 shown)

14.2 QPI Write Operation(s)

QPI Writes can be done by issuing the command ‘h82: Masking only applicable when MR0[7]=0.

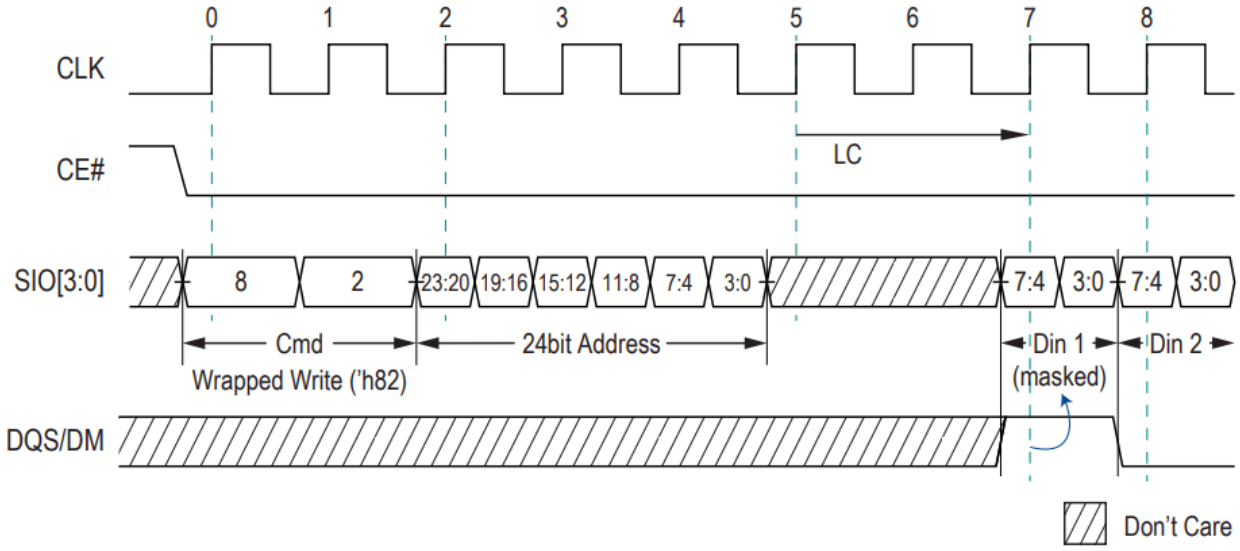


Figure 10: QPI Write ‘h82 (Latency Code 2 shown)

15 Reset Operation

The Reset operation is used to puts the device back to its default mode after power-up. This is a 2-step operation which consists of two commands: Reset-Enable (RSTEN) and Reset(RST).

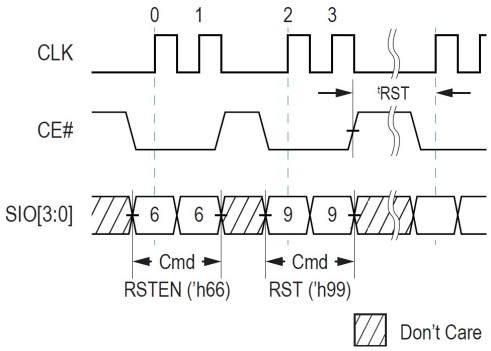


Figure 11: QPI Reset

Reset command has to immediately follow the Reset-Enable command in order for reset operation to take effect. Any command other than the Reset command after the Reset-Enable command will cause the device to exit Reset-Enable state and abandon reset operation.

16 Input/Output Timing

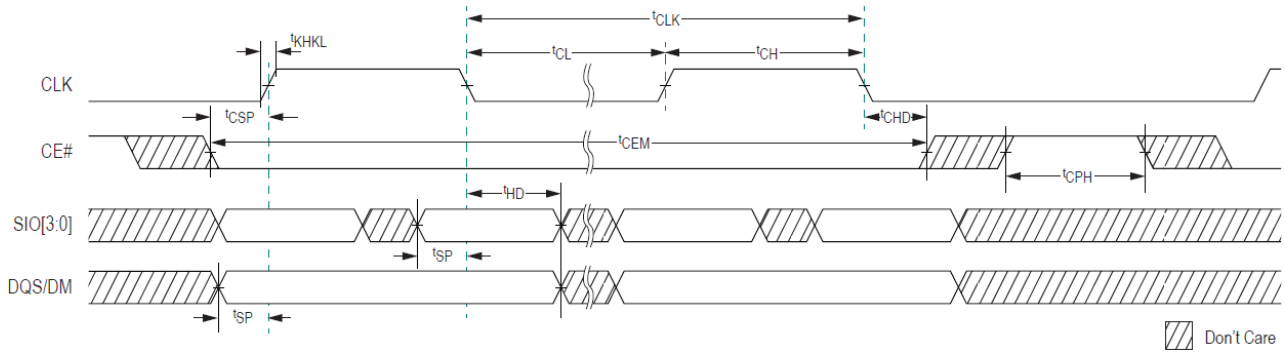


Figure 12: Input Timing

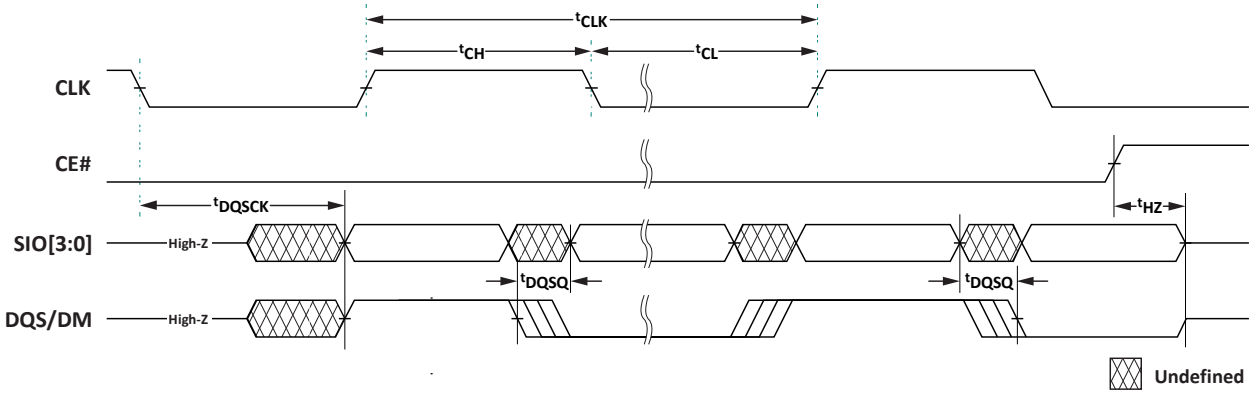


Figure 13: Output Timing

17 Electrical Specifications:

17.1 Absolute Maximum Ratings

Table 8: Absolute Maximum Ratings

Parameter	*Symbol*	*Rating*	*Unit*	*Notes*
Voltage to any ball except V_{DD} relative to V_{SS}	VT	-0.4 to V_{DD}/+0.4	V	
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.4 to +2.45	V	
Storage Temperature	T_{STG}	-55 to +150	°C	1

Notes 1: Storage temperature refers to the case surface temperature on the center/top side of the PSRAM.

Caution:
Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

17.2 Input Signal Overshoot

During DC conditions, input or I/O signals should remain equal to or between VSS and VDD. During voltage transitions, inputs or I/Os may negative overshoot VSS to -1.0V or positive overshoot to VDD +1.0V, for periods up to 20 ns.

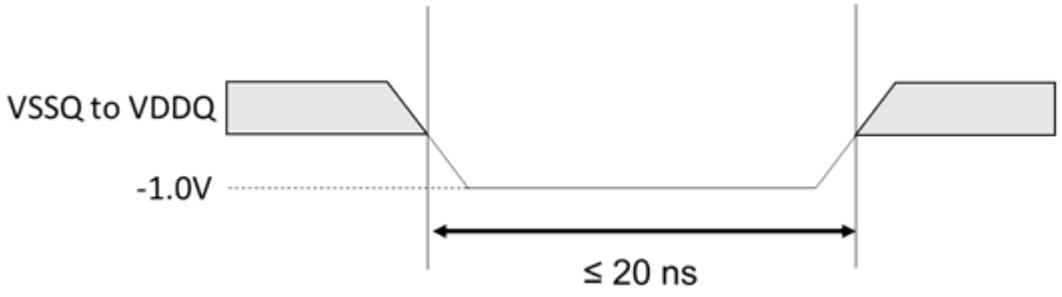


Figure 14 Maximum Negative Overshoot Waveform

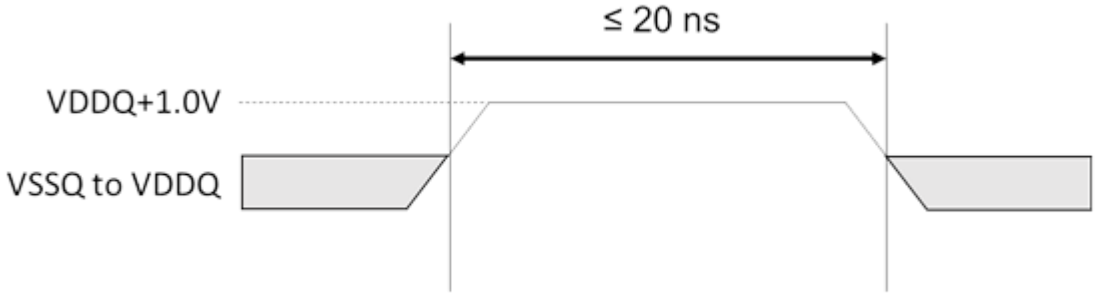


Figure 15 Maximum Positive Overshoot Waveform

17.3 Pin Capacitance

Table 9: Bare Die Pin Capacitance

Parameter	Symbol	Min	Max	Unit	Notes
Input Pin Capacitance	CIN		2	pF	VIN=0V
Output Pin Capacitance	COUT		3	pF	VOUT=0V

Note: spec'd at 25°C.

Table 10: Package Pin Capacitance

Parameter	Symbol	Min	Max	Unit	Notes
Input Pin Capacitance	CIN		6	pF	VIN=0V
Output Pin Capacitance	COUT		8	pF	VOUT=0V

Note: spec'd at 25°C.

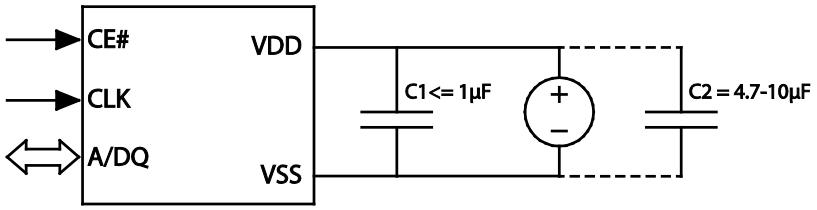
Table 11: Load Capacitance

Parameter	Symbol	Min	Max	Unit	Notes
Load Capacitance	C_L		15	pF	

Note: System C_L for the use of package

17.4 Decoupling Capacitor Requirement

System designers need to take care of power integrity considering voltage regulator response and the memory peak currents/usage modes.



17.4.1 Low ESR cap C1:

It is recommended to place a low ESR decoupling capacitor of <=1µF close to the device to absorb transient peaks.

17.4.2 Large cap C2:

Though Halfsleep™ average current is small (less than 100µA), its peak current from internal periodical burst refresh can reach up to the level of 25mA. The peak current duration can last for few tens of microseconds. During this period if the system regulator cannot supply such large peaks, it is important to place a 4.7µF-10µF cap to cover the burst refresh current demand and replenish the cap before the next burst of refresh.

If needed, contact AP Memory for further decoupling solution assistance.

17.5 Operating Conditions

Table 12: Operating Characteristics

Parameter	*Min*	*Max*	*Unit*	*Notes*
Operating Temperature (extended)	-40	105	°C	
Operating Temperature (standard)	-40	85	°C	

17.6 DC Characteristics

Table 13: DC Characteristics

Symbol	*Parameter*	*Min*	*Max*	*Unit*	*Notes*
V_{DD}	Supply Voltage	1.62	1.98	V	
V_{IH}	Input high voltage	V_{DD}-0.4	V_{DD}+0.2	V	
V_{IL}	Input low voltage	-0.2	0.4	V	
V_{OH}	Output high voltage (I_{OH}=-0.2mA)	0.8 V_{DD}		V	
V_{OL}	Output low voltage (I_{OL}=+0.2mA)		0.2 V_{DD}	V	
I_{LI}	Input leakage current		1	µA	
I_{LO}	Output leakage current		1	µA	
I_{CC}	Read/Write (166Mhz)		15	mA	1,2
I_{CC}	Read/Write (133Mhz)		13	mA	1,2
I_{CC}	Read/Write (66Mhz)		8	mA	1,2
ISB_{EXT}	Standby current (105C)		590	µA	3
ISB_{STD}	Standby current (85C)		420	µA	3

Note 1: Output load current not included.

2: 50% bus toggling rate.

3: Standby current is measured when CLK is in DC low state.

4: Typical $ISB_{STDROOM}$ is 64µA.

5: Typical ISB_{STD_HS} is 19.5µA.

17.7 AC Characteristics

Table 14: READ/WRITE Timing

Symbol	*Parameter*	*Min*	*Max*	*Unit*	*Notes*
^{t}CLK	CLK period SIP	6		ns	166MHz*
^{t}CH/^{t}CL	Clock high/low width	0.45	0.55	^{t}CLK(min)	
^{t}KHKL	CLK rise or fall time		0.8	ns	1
^{t}CPH	CE# HIGH between subsequent burst operations	20		ns	
^{t}CEM	CE# low pulse width (excluding Halfsleep™ Exit)		8	µs	Standard temp
			3	µs	Extended temp
^{t}CSP	CE# setup time to CLK rising edge (CE# low)	2		ns	
^{t}CSP2	CE# setup time to CLK rising edge (CE# high)	1		ns	
^{t}CHD	CE# hold time from CLK falling edge SIP	0.5		ns	
	CE# hold time from CLK falling edge PKG	0.5		ns	
^{t}CHD_HS	CE# hold time from CLK rising edge for	6		ns	
^{t}SP	Setup time to active CLK edge	0.8		ns	
^{t}HD	Hold time from active CLK edge	0.8		ns	
^{t}RPRE	DQS read preamble	1.5		^{t}CLK	
^{t}DQSCK	DQS output access time from CLK	2	7	ns	
^{t}HS	Minimum Halfsleep™ duration	150		µs	
^{t}XHS	Halfsleep™ Exit CE# low to CLK setup time	150		µs	
^{t}XPHS	Halfsleep™ Exit CE# low pulse width	60		ns	
			tCEM	µs	
^{t}RST	Time between end of RST CMD to next valid CMD	50		ns	

Note 1: Measured from 20% to 80% V_{DD}.

18 Change Log

Version	Who	Date	Description
0.1	Kim/ Gene/ Eric	Jun 20, 2022	Initial Version derived from E8 SQPI DDR
0.2	Kim	July 25, 2022	Add ICC max current at difference frequency.
1.0	Kim	July 17, 2023	Remove tQH from Figure 13: Output Timing
1.1	Kim	Nov 30, 2023	Modify Standby and Halfsleep typical current Add chapter 17.2 Input signal overshoot