# Octal Double-Data-Rate PSRAM

## Specifications

- Single Supply Voltage:
  - $V_{DD}$ =1.62 to 1.98V
  - $V_{DDQ}$ =1.62 to 1.98V
- Interface: Octal SPI with DDR mode, two bytes transfers per one clock cycle
- Performance: Clock rate up to 200MHz, 400MBps read/write throughput
- Organization: 256Mb, 32M x 8bits with 2048 bytes per page
  - Column address: AY0 to AY10
  - Row address: AX0 to AX13
- Refresh: Self-managed
- Operating temperature range
  - Tc= -40°C to +85°C (standard range)
  - Tc = -40°C to +105°C (extended range)
- Typical mean Room Standby Current:
  - 40µA @ 25°C (Halfsleep™ Mode with data retained)
- Maximum Standby Current:
  - 1100µA @ 105°C
  - 680µA @ 85°C

## o Features

- Low Power Features:
  - Auto Temperature Compensated Self-Refresh (ATCSR) by built-in temperature sensor
  - Ultra Low Power Halfsleep™ mode with data retention.
- Software reset
- Reset pin available
- Output driver LVCMOS with programmable drive strength
- Data mask (DM) for write data
- Data strobe (DQS) enabled high speed read operation
- Register configurable write and read initial latencies
- Write burst length, maximum 2048 Byte, minimum 2 Byte.
- Wrap & hybrid burst in 16/32/64/128 lengths.
- Linear Burst Command (wraps at page boundary)
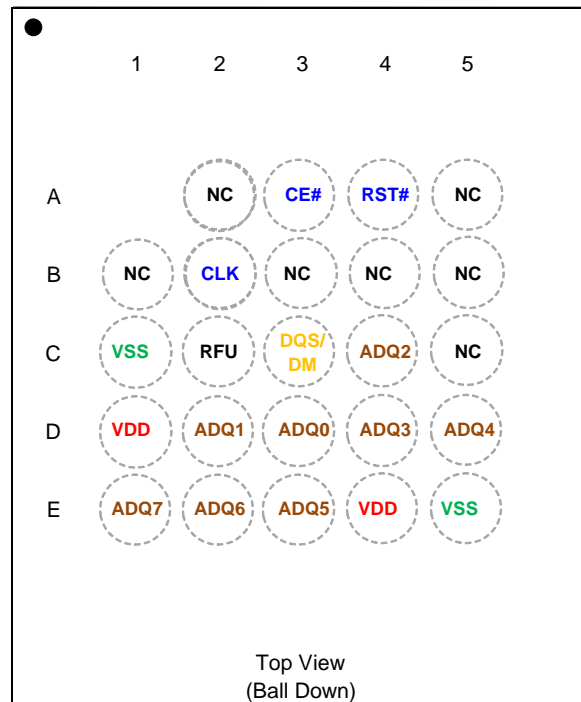
# Table of Contents

## 1 Table of Contents

## 2 Package Information

### 2.1 Package Types : BGA 24B x8 (BD)

The APS25608N-OCHx is available in mini-BGA 24B package 6 x 8 x 1.2mm, ball pitch 1.0mm, ball size 0.4mm, package code "BD".

- Ball Assignment for MINI-BGA 24B

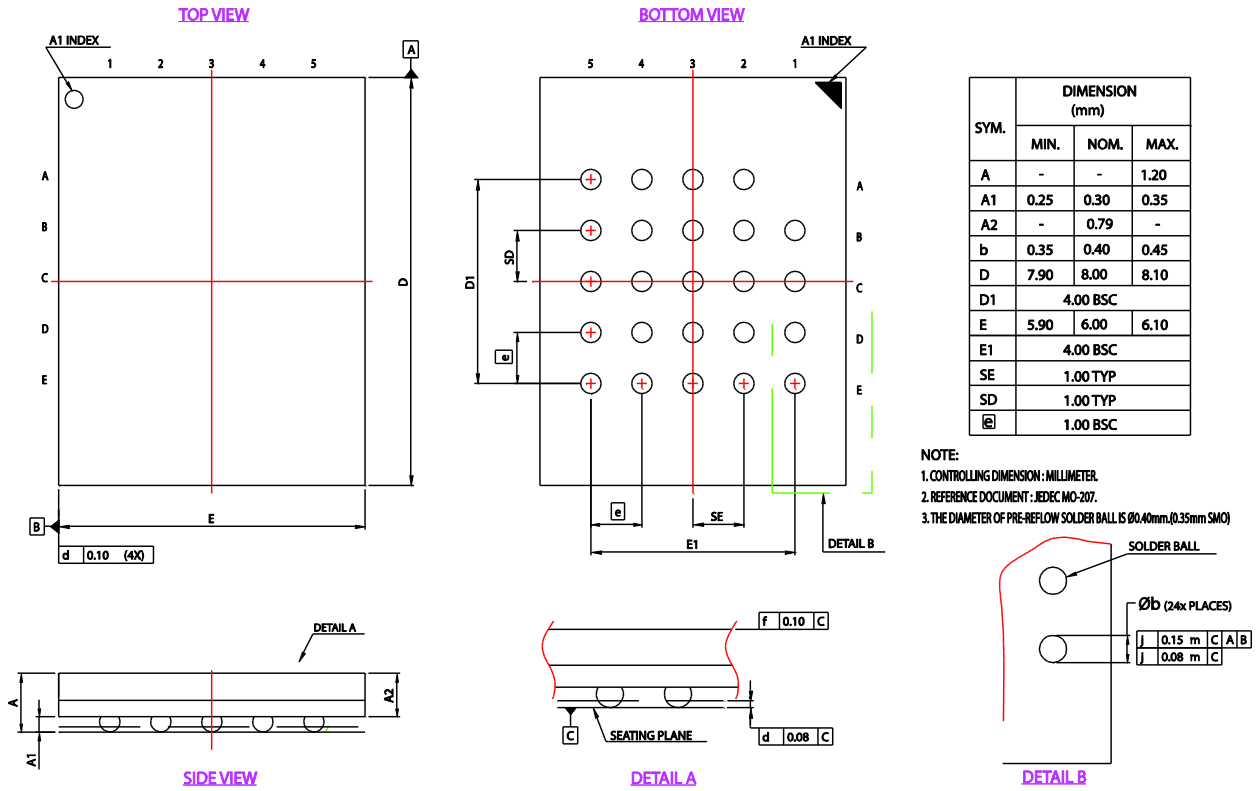|   | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|
| A |  | NC | CE# | RST# | NC |
| B | NC | CLK | NC | NC | NC |
| C | VSS | RFU | DQS/DM | ADQ2 | NC |
| D | VDD | ADQ1 | ADQ0 | ADQ3 | ADQ4 |
| E | ADQ7 | ADQ6 | ADQ5 | VDD | VSS |

Top View
(Ball Down)

(6x8x1.2mm)(P1.0)(B0.4)

Note:

1. Part Number APS25608N-OCHx-BD for 256Mb

2. RFU stands for Reserved for Future Use, which shall be left floating

3. NC: No internal connection.

## 2.2 Package Outline Drawing

### 2.2.1 BGA 24B x8 , package code BD



TOP VIEW

BOTTOM VIEW

SIDE VIEW

DETAIL A

DETAIL B

| SYM. | DIMENSION (mm) | | |
|------|------|------|------|
| | MIN. | NOM. | MAX. |
| A | - | - | 1.20 |
| A1 | 0.25 | 0.30 | 0.35 |
| A2 | - | 0.79 | - |
| b | 0.35 | 0.40 | 0.45 |
| D | 7.90 | 8.00 | 8.10 |
| D1 | 4.00 BSC | | |
| E | 5.90 | 6.00 | 6.10 |
| E1 | 4.00 BSC | | |
| SE | 1.00 TYP | | |
| SD | 1.00 TYP | | |
| e | 1.00 BSC | | |

NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.
3. THE DIAMETER OF PRE-REFLOW SOLDER BALL IS Ø0.40mm.(0.35mm SMO)

SOLDER BALL

Øb (24x PLACES)

## 3    Ordering Information

**Table 1:  Ordering Information**

| Part Number | IO | Temperature Range | Max Frequency | Note |
|---|---|---|---|---|
| APS25608N-OCH-BD | X8 | Tc = -40°C to +85°C | 200 MHz | BGA 24B |
| APS25608N-OCHX-BD | X8 | Tc = -40°C to +105°C | 200 MHz | BGA 24B |

Note for "x"
- -OCH is standard part. PN example of 24B BGA is APS25608N-OCH-BD for normal temperature grade.

| A | P | S | 256 | 08 | N | ── | | OC | H | | | ── | BD |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|

Type:
P: PSRAM    Density    Vendor define    Protocol    Temp grade    Package code

Company    Product:    Width    Voltage    Special feature    Reserved    RDL/Bump:
S: Sync                                                                          Only with RDL or Bump
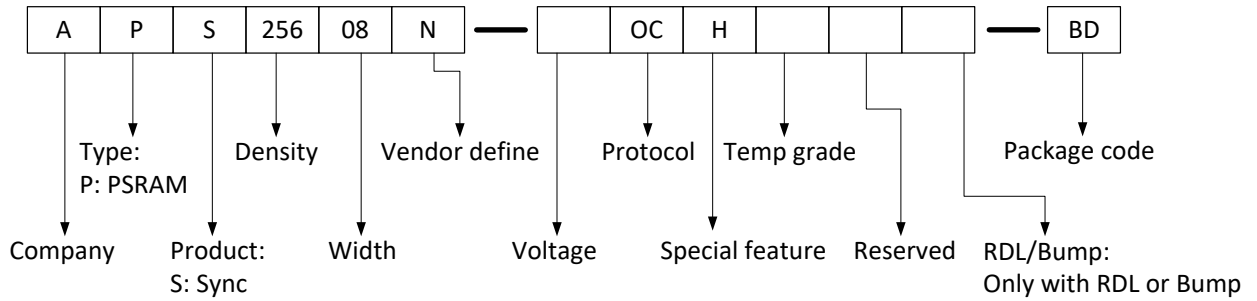
## 4    Signal Table

All signals are listed in Table 2.

**Table 2: Signals Table**

| Symbol | Type | Description | Comments |
|---|---|---|---|
| $V_{DD}$ | Power | Core & IO supply 1.8V | $V_{DDQ}$ short to $V_{DD}$ internally. |
| $V_{SS}$ | Ground | Core& IO supply ground | |
| A/DQ[7:0] | IO | Address/DQ bus [7:0] | |
| DQS/DM<0> | IO | DQ strobe clock for DQ[7:0] during all reads, Data mask for DQ[7:0]  during memory writes.  DM is active high.  DM=1 means "do not write". | |
| CE# | Input | Chip select, active low. When CE#=1, chip is in standby state. | |
| CLK | Input | Clock signal | |
| RESET# | Input | Reset signal, active low.  Optional, as the pad is internally tied to a weak pull-up and can be left floating. | May not be available for all package types |

## 5    Block diagram
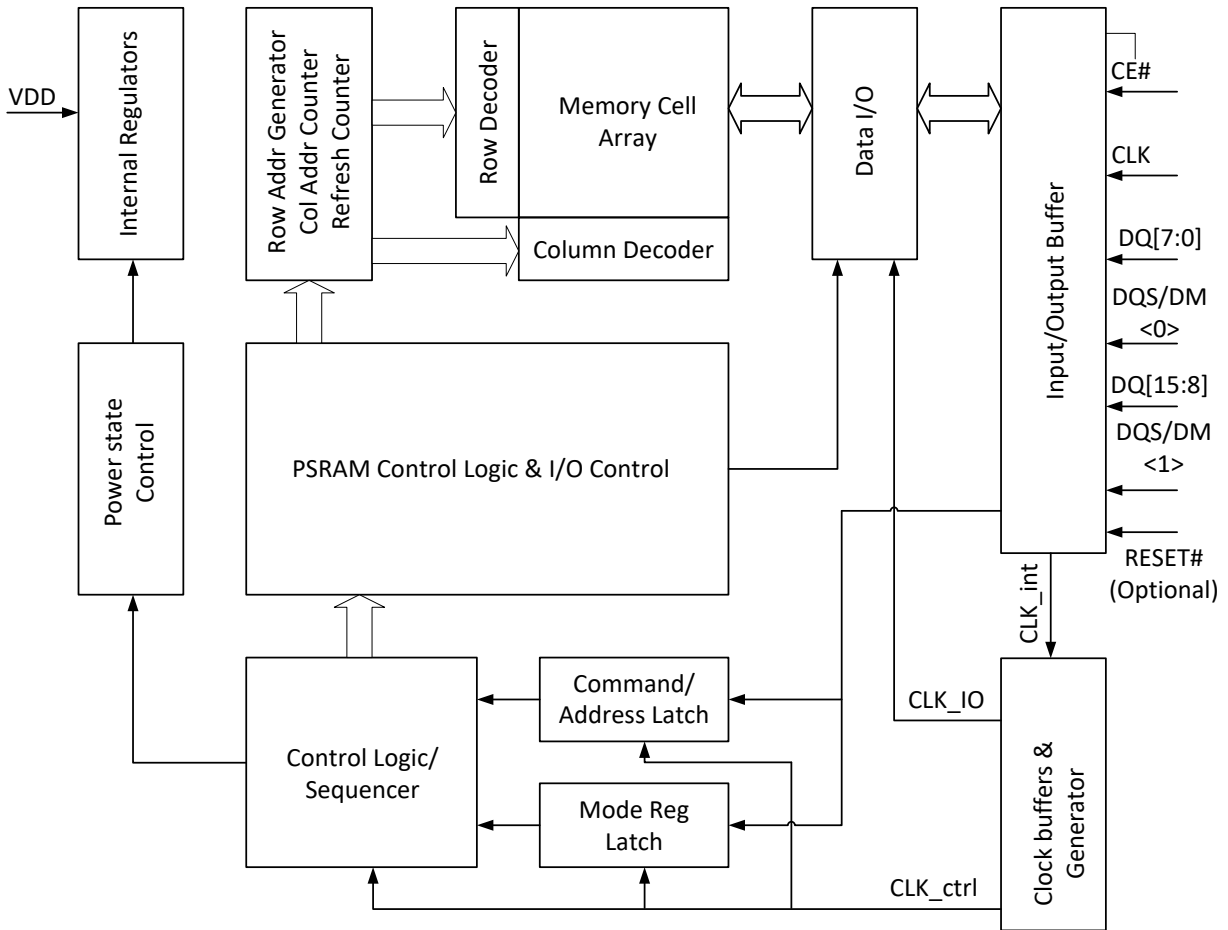
# 6 Power-Up Initialization

Octal DDR products include an on-chip voltage sensor used to start the self-initialization process. $V_{DD}$ and $V_{DDQ}$ must be applied simultaneously. When they reach a stable level at or above minimum $V_{DD}$, the device is in Phase 1 and will require 150µs to complete its self-initialization process. The user can then proceed to Phase 2 of the initialization described in sections 1.1

During Phase 1 CE# should remain HIGH (track $V_{DD}$ within 200mV); CLK should remain LOW.

After Phase 2 is complete the device is ready for operation, however Halfsleep™ entry and Deep Power Down (DPD) entry are not available until Halfsleep™ Power Up (tHSPU) or DPD Power Up (tDPDp) durations are observed.

## 6.1 Power-Up Initialization Method 2 (via. Global Reset)

As an alternate power-up initialization method, after the Phase 1 150µs period the Global Reset command can also be used to reset the device in Phase 2 as follows:
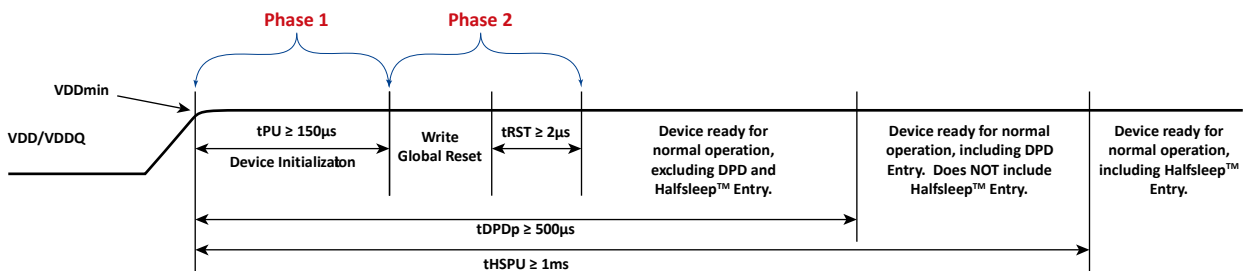
**Figure 1. Power-Up Initialization Method 2 Timing with Global Reset**

The Global Reset command resets all register contents. Memory content is not guaranteed. The command frame is 4 clocked CE lows. The Global Reset command sequence is shown below.
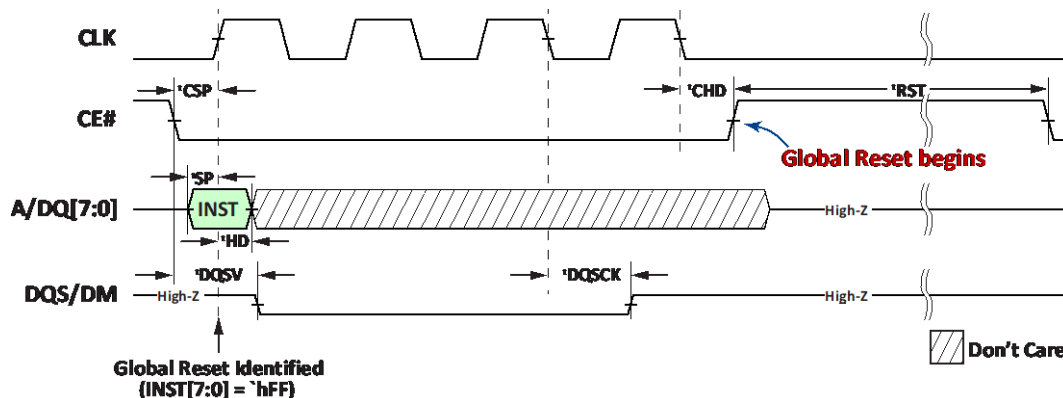
**Figure 2: Global Reset**

## 7    Interface Description

### 7.1    Address Space

Octal DDR PSRAM device is byte-addressable. Memory accesses are required to start on even addresses (A[0]='0').

### 7.2    Burst Type & Length

Read and write operations are always in wrap mode within 16, 32, 64, 128 or 2K (see Table 9).  Bursts can start on any even address.  Write Burst Length has a minimum of 2 bytes (1 rising CLK and 1 falling CLK edge).  Read has no minimum length.  Both write and read have no restriction on maximum Burst Length as long as tCEM is met.

### 7.3    Command/Address Latching

After CE# goes LOW, instruction code is latched on $1^{st}$ CLK rising edge.  Row Access (RA) address is latched on the $3^{rd}$ & $4^{th}$ edges ($2^{nd}$ CLK rising edge, $2^{nd}$ CLK falling edge), while Column Access (CA) address is latched on the $5^{th}$ & $6^{th}$ CLK edges ($3^{rd}$ CLK rising edge, $3^{rd}$ CLK falling edge).

| Pin | 1st CLK | | 2nd CLK | | 3rd CLK | |
|---|---|---|---|---|---|---|
| A/DQ[7] | INST[7] | × | rsvd. | RA[6] | CA[9] | rsvd. |
| A/DQ[6] | INST[6] | × | RA[13] | RA[5] | CA[8] | rsvd. |
| A/DQ[5] | INST[5] | × | RA[12] | RA[4] | CA[7] | rsvd. |
| A/DQ[4] | INST[4] | × | RA[11] | RA[3] | CA[6] | rsvd. |
| A/DQ[3] | INST[3] | × | RA[10] | RA[2] | CA[5] | CA[3] |
| A/DQ[2] | INST[2] | × | RA[9] | RA[1] | CA[4] | CA[2] |
| A/DQ[1] | INST[1] | × | RA[8] | RA[0] | rsvd. | CA[1] |
| A/DQ[0] | INST[0] | × | RA[7] | CA[10] | rsvd. | CA[0] |

Remarks:          × = don't care ($V_{IH}/V_{IL}$)

During the Command/Address cycles (first three clocks) DQS/DM will be driven low by the PSRAM for all operations.

## 7.4 Command Truth Table

The Octal DDR PSRAM recognizes the following commands specified on the INST (Instruction) cycle defined by the Address/DQ pins.

| Command | 1st CLK | | 2nd CLK | | 3rd CLK | |
|---|---|---|---|---|---|---|
| Sync Read | 80h | × | A3 | A2 | A1 | A0 |
| Sync Write | 00h | × | A3 | A2 | A1 | A0 |
| Sync Read (Linear Burst) | A0h | × | A3 | A2 | A1 | A0 |
| Sync Write (Linear Burst) | 20h | × | A3 | A2 | A1 | A0 |
| ID Register Read | C0h or E0h | × | 00h | 00h | 00h | 00h |
| Mode Register Read | C0h or E0h | × | 00h | 04h | 00h | 00h |
| Mode Register Write | 40h or 60h | × | 00h | 04h | 00h | 00h |
| Halfsleep<sup>TM</sup> Entry | 40h or 60h | × | 00h | 04h | 00h | 06h |
| Global Reset | FFh | | | × | | |

Remarks: × = don't care ($V_{IH}/V_{IL}$)

A3 = RA[max:7], unused address bit is reserved

A2 = {RA[6:0],CA[10]}

A1 = {CA[9:4], 2xRsvd.}, unused address bits are reserved

A0 = {4xRsvd., CA[3:0]}

MA = Mode Register Address

Notes: 1) Default Burst Type set in Mode Register is 32 Byte Wrap

## 7.5 Read Operation

After address latching, the device initializes DQS/DM to '0 from CLK rising edge of the 3$^{rd}$ clock cycle (A1).  See Figure 3 below.

Output data is available after LC cycles, as shown in Figure 4 & Figure 5, LC is latency configuration code as defined in Table 5 and Table 6.  When data is valid, A/DQ[7:0] and DQS/DM follow the timing specified in Figure 6.  Synchronous timing parameters are shown in Table 11 & Table 12.

In case of internal refresh insertion, variable latency output data is delayed by (LCx2) latency cycles as shown in Figure 4.  The 1$^{st}$ DQS/DM rising edge after read pre-amble will indicate the beginning of valid data.

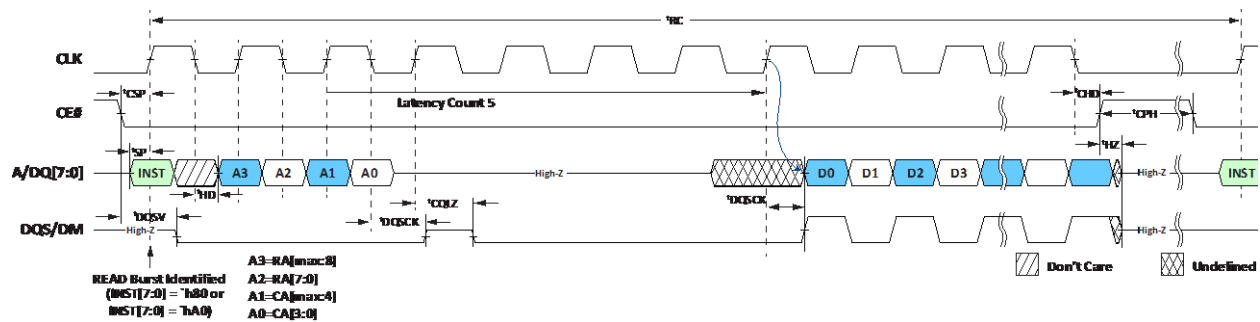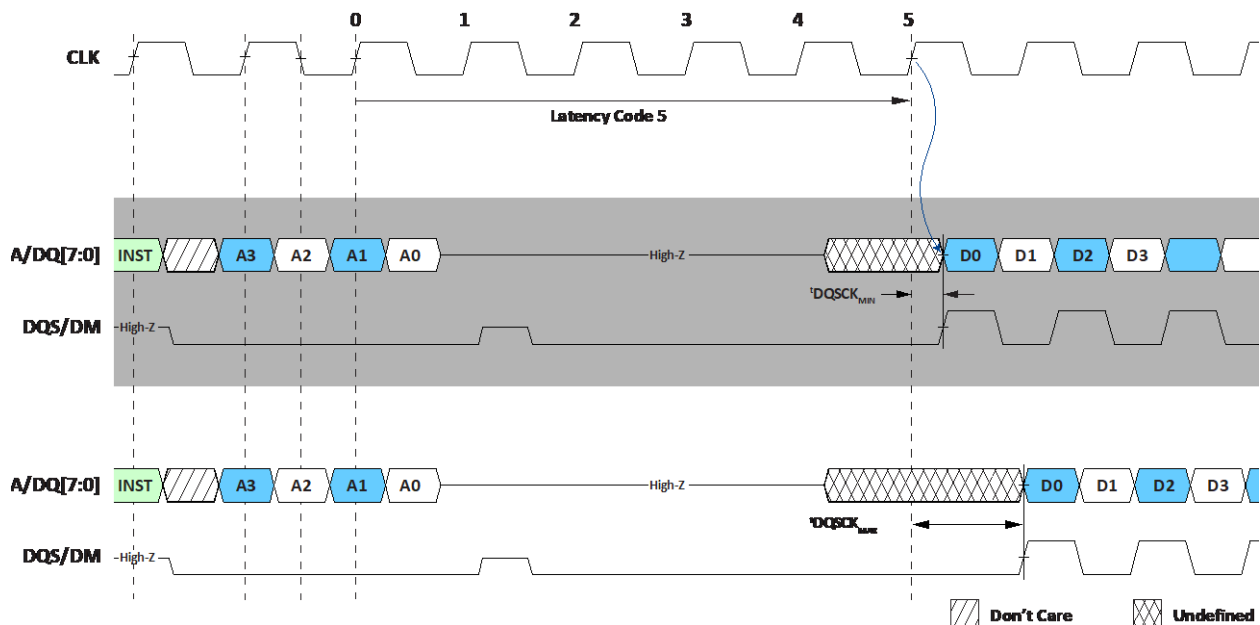

**Figure 3: Synchronous Read**



**Figure 4: Variable Read Latency Refresh Pushout**
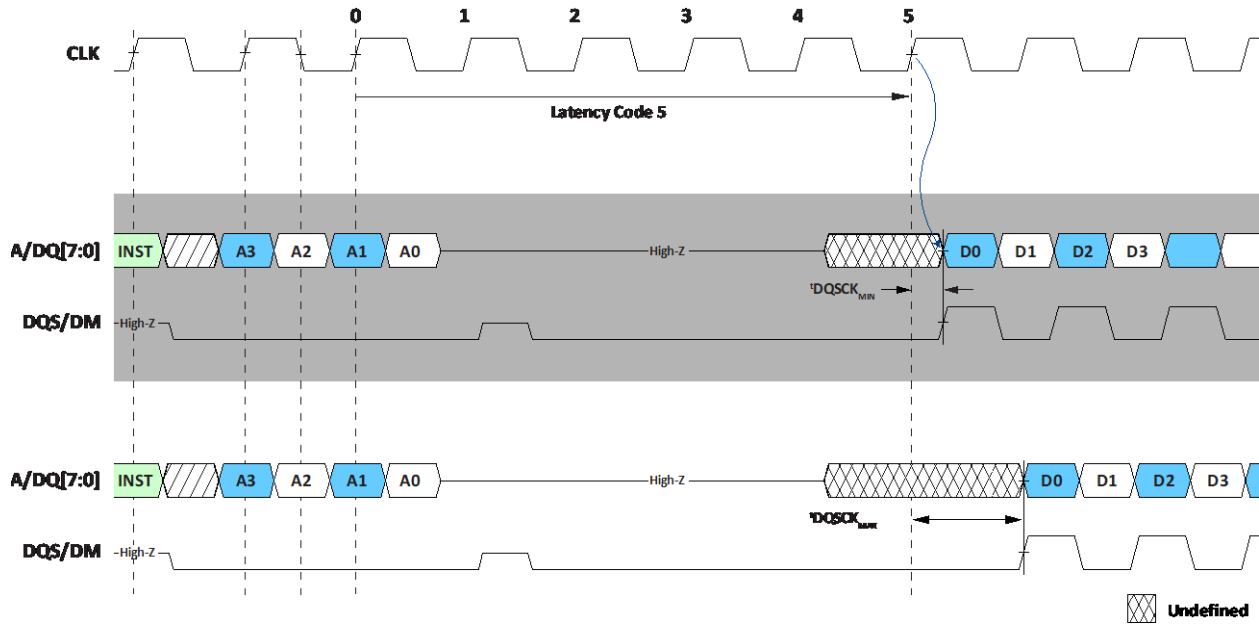
**Figure 5: Read Latency & tDQSCK**
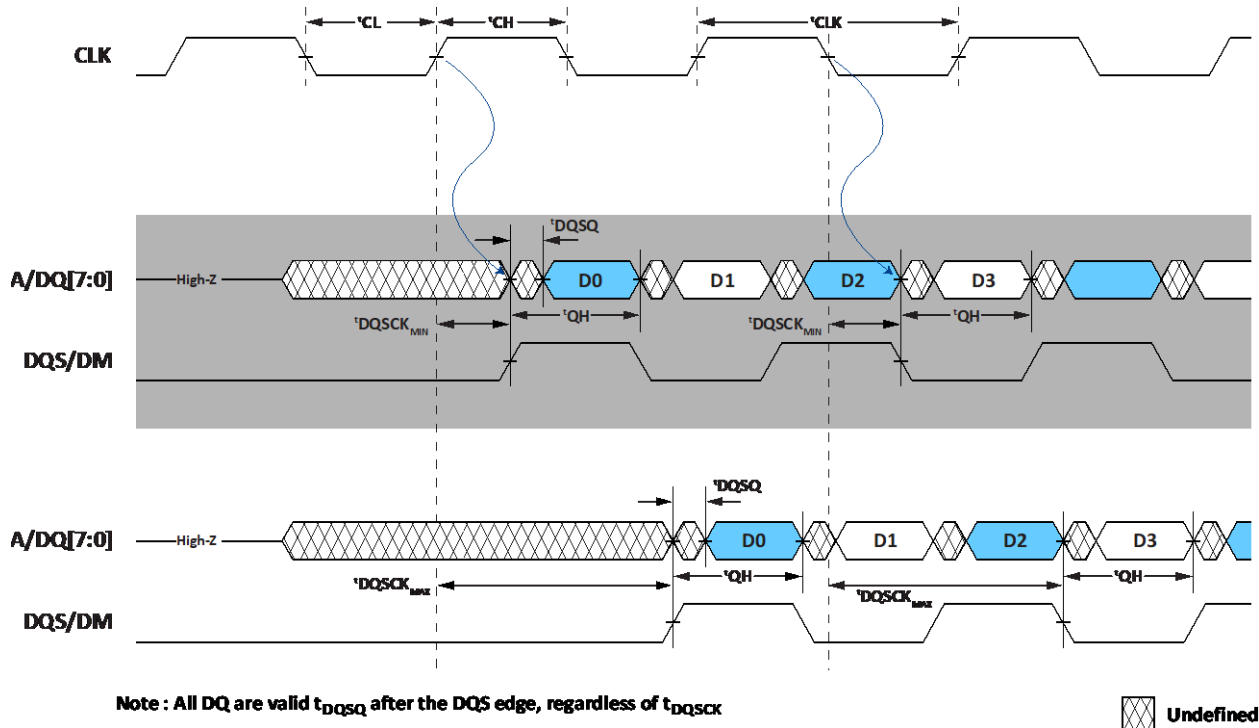


Note : All DQ are valid $t_{DQSQ}$ after the DQS edge, regardless of $t_{DQSCK}$

**Figure 6: Read DQS/DM & DQ timing**

## 7.6 Write Operation

A minimum of 2 bytes of data must be input in a write operation.  In the case of consecutive short burst writes, tRC must be met by issuing additional CE# high time between operations.  Single-byte write operations can be performed by masking the un-written byte with DQS/DM as shown in Figure 7.
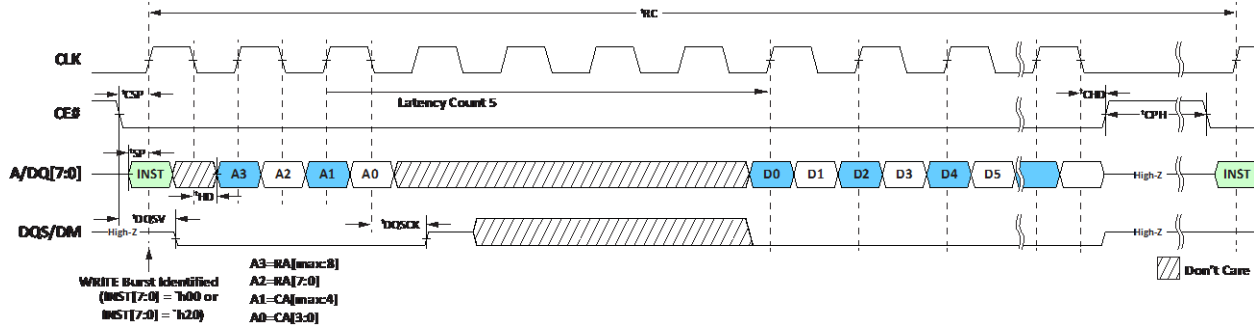
**Figure 7: Synchronous Write Unmasked Example**
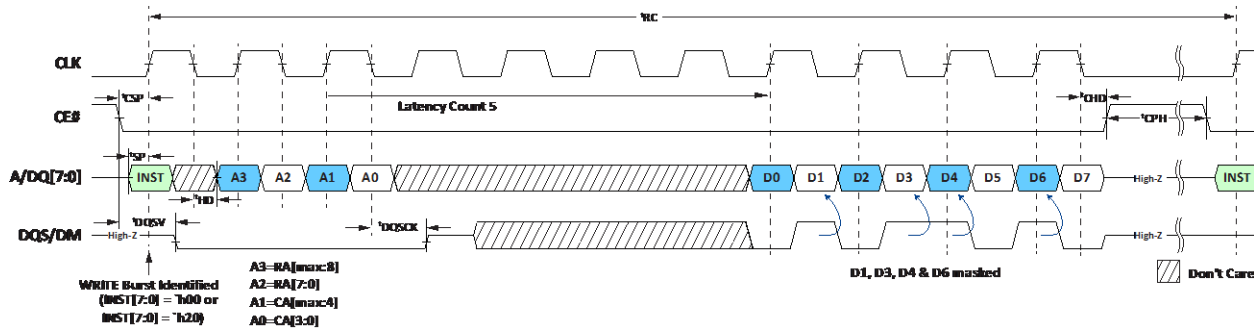
**Figure 8: Synchronous Write Masking Example**
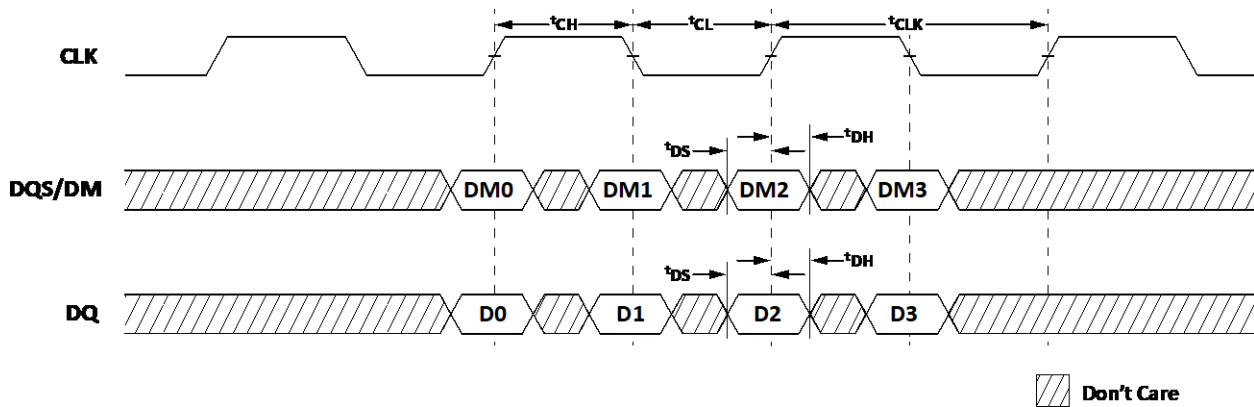
**Figure 9: Write DQS/DM & DQ Timing**

## 7.7 Control registers

Register Read is shown below. Register reads are <u>always</u> LC latency cycles. Register Address in command determines which Register is read from.
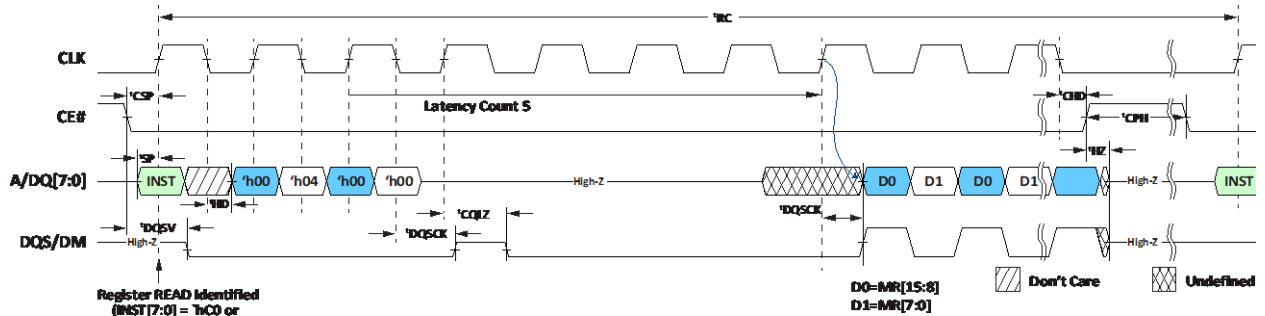


**Figure 10: Mode Register Read**
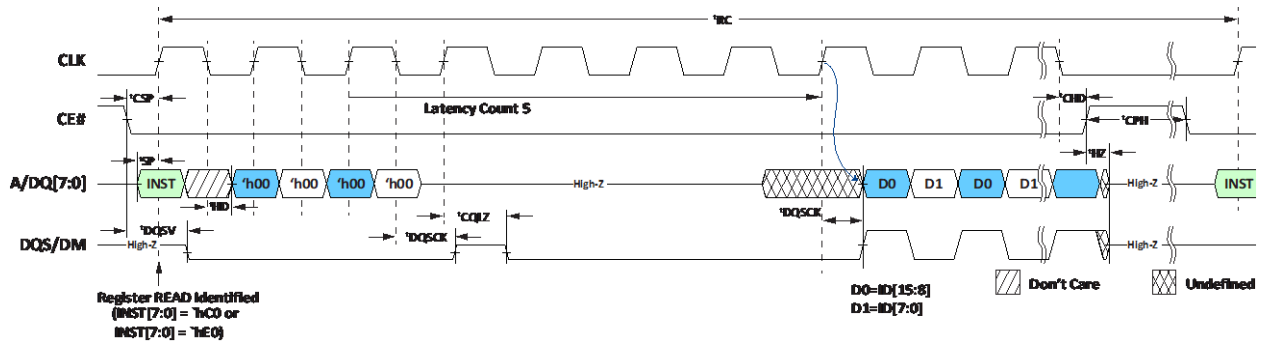


**Figure 11: ID Register Read**

Register Write is shown below.  Register Writes are <u>always</u> 0 latency cycle.
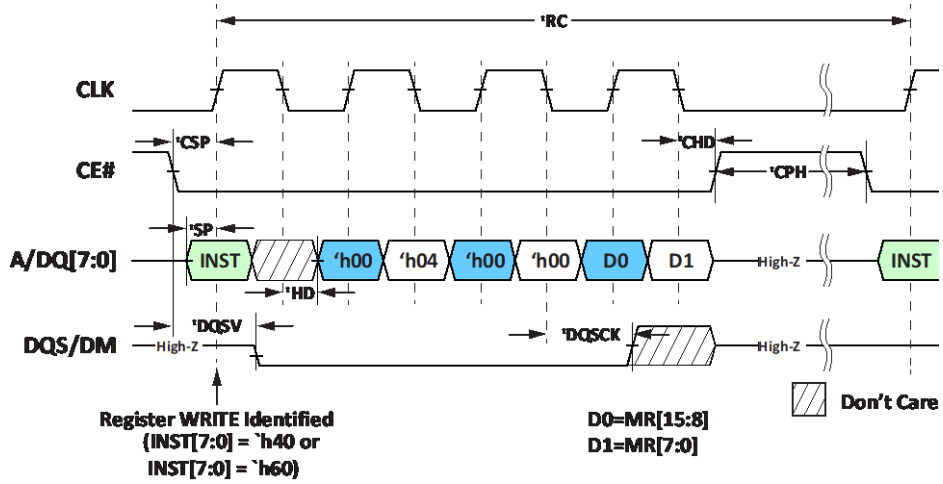


**Figure 12: Register Write**

ID & Mode Register mappings are shown in Table 3 & Table 4.

**Table 3: ID Register Table**

| Bit | Purpose | Settings |
|---|---|---|
| 15 | KBD | 0 - Good Die<br>1 - Known Bad Die |
| 14-13 | reserved | 00 |
| 12-8 | Row Address MSB | 01101 - 14 row address bits (128M), 13 logical row address<br>01110 - 15 row address bits (256M), 14 logical row address*<br>01111 - 16 row address bits (512M), 15 logical row address |
| 7-4 | Col Address MSB | 1001 - 10 column address bits, 11 logical column address* |
| 3-0 | Vendor | 1101 - AP Memory |

*Please refer section 7.3 Command/Address Latching, 15 row address bits of 256Mb includes 14 logical row address and 1 logical column address.

**Table 4: Mode Register Table**

| Bit | Purpose | Settings |
|---|---|---|
| 15 | Deep Power Down Enable | 0 - Deep Power Down Entry<br>1 - Normal Operation (default) |
| 14-12 | Drive Strength | see Table 7 |
| 11-10 | Refresh Rate | see Table 8 |
| 9-8 | | reserved |
| 7-4 | Latency Code | see Table 5&6 |
| 3 | Latency Type | 0 - Variable Latency (default)<br>1 - Fixed Latency |
| 2 | Burst Type | 0 - Wrapped (default)<br>1 - Hybrid Continuous |
| 1-0 | Burst Length | 00 - 128 bytes<br>01 - 64 bytes<br>10 - 32 bytes (default)<br>11 - 16 bytes |

**Table 5: Latency Configuration Codes MR[7:4]**

| | VL Codes (MR[3]=0) | | FL Codes (MR[3]=1) | Max Input CLK Freq (MHz) | |
|---|---|---|---|---|---|
| MR[7:4] | No Refresh (LC) | Refresh (LCx2) | (LCx2) | Standard | Extended |
| 0000 | 3 | 6 | 6 | 66 | 66 |
| 0001 | 4 | 8 | 8 | 104 | 104 |
| 0010 | 5 | 10 | 10 | 133 | 133 |
| 0011 | 6 | 12 | 12 | 166 | 166 |
| 0100 | 7 | 14 | 14 | 200 | 200 |
| 0101 | 8 (default) | 16 | 16 | 200 | 200 |
| others | Reserved | - | - | - | - |

**Table 6: Operation Latency Code Table**

| Type | Operation | VL (default) | | FL |
|---|---|---|---|---|
| | | No Refresh | Refresh | |
| Memory | Read | LC | LCx2 | LCx2 |
| | Write | LC | | LC |
| Register | Read | LC | | LC |
| | Write | 0 | | 0 |

**Table 7: Drive Strength Codes MR [14:12]**

| Codes | Drive Strength |
|---|---|
| '000 | 100Ω |
| '001 | 66Ω |
| '010 | 50Ω |
| '011 | 40Ω |
| '100 | 33Ω |
| '101 | 33Ω |
| '110 | 25Ω |
| '111 | 25Ω (default) |

**Table 8: Refresh Frequency setting MR[11:10]**

| MR[11:10] | Refresh Frequency |
|---|---|
| x0 | Always 4x Refresh (default) |
| 01 | Enables 1x Refresh when temperature allows |
| 11 | Enable 0.5x Refresh when temperature allows |

Note: x= don't care

**Table 9: Burst Type MR[2], Burst Length MR[1:0], & Linear Burst**

By default the device powers up in 32 Byte Wrap. In non-Hybrid burst (MR[2]=0), MR[1:0] sets the burst address space in which the device will continually wrap within. If Hybrid Burst Wrap is selected (MR[2]=1), the device will burst through the initial wrapped Burst Length once, then continue to burst incrementally up to maximum column address (2K) before wrapping around within the entire column address space. Burst Length (MR[1:0]) can be set to 16,32,64 & 128 bytes.

| MR[2] | MR [1:0] | Burst Length | Example of Sequence of Bytes During Wrap | |
|---|---|---|---|---|
| | | | Starting Address | Byte Sequence |
| '0 | '00 | 128 Byte Wrap | 4 | [4,5,6,...127,0,1,2,...] |
| '0 | '01 | 64 Byte Wrap | 4 | [4,5,6,...63,0,1,2,...] |
| '0 | '10 | 32 Byte Wrap (default) | 4 | [4,5,6,...31,0,1,2,...] |
| '0 | '11 | 16 Byte Wrap | 4 | [4,5,6,...15,0,1,2,...] |
| '1 | '00 | 128 Byte Hybrid Wrap | 2 | [2,3,4,...127,0,1],128,129...2047,0,1,... |
| '1 | '01 | 64 Byte Hybrid Wrap | 2 | [2,3,4,...63,0,1],64,65,66,...2047,0,1,... |
| '1 | '10 | 32 Byte Hybrid Wrap | 2 | [2,3,4,...31,0,1],32,33,34,...2047,0,1,... |
| '1 | '11 | 16 Byte Hybrid Wrap | 2 | [2,3,4,...15,0,1],16,17,18,...2047,0,1,... |

The Linear Burst Command (INST[5:0]=6'b10_0000) forces the current array read or write to do 2K Byte Wrap. The burst continues linearly from the starting address and at the end of the page it wraps back to the beginning of the page. This special burst instruction can be used on both array writes and reads. A new command is needed to access a different page.

## 7.8 Deep Power Down Mode

Deep Power Down Mode (DPD) is a feature which puts the device in an ultra-low power state. DPD Mode Entry is entered by using Register Write to write a 0 into MR[15]. CE# going high initiates the DPD Mode and must be maintained for the minimum duration of tDPD. The Deep Power Down Entry command sequence is shown below.



**Figure 13: Deep Power Down Entry Write**

Deep Power Down Exit is initiated by a low pulsed CE# or RESET#. After a CE# DPD exit, CE# must be held high until the first operation begins (observing minimum tXDPD).
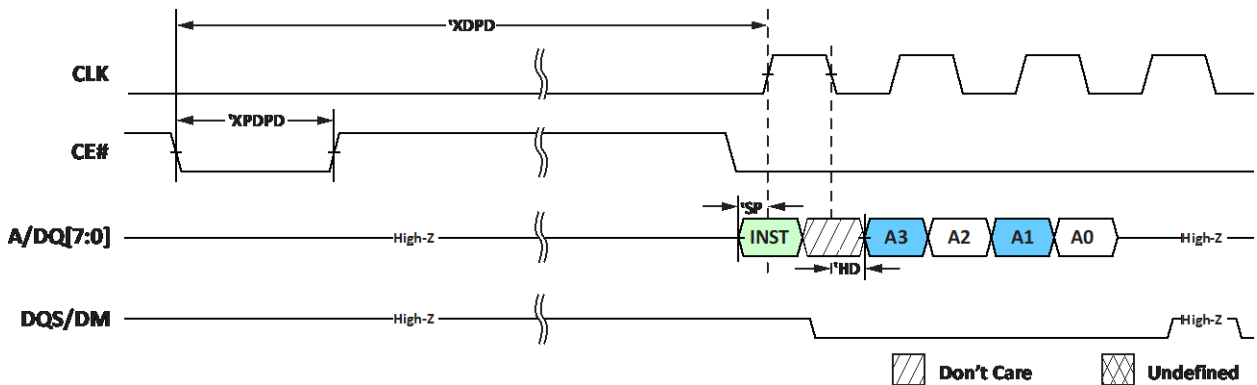


**Figure 14: Deep Power Down Exit with CE# (Read Operation shown as example)**

After a RESET# DPD exit, CE# and RESET# must be held high until the first operation begins (observing minimum tRCH).
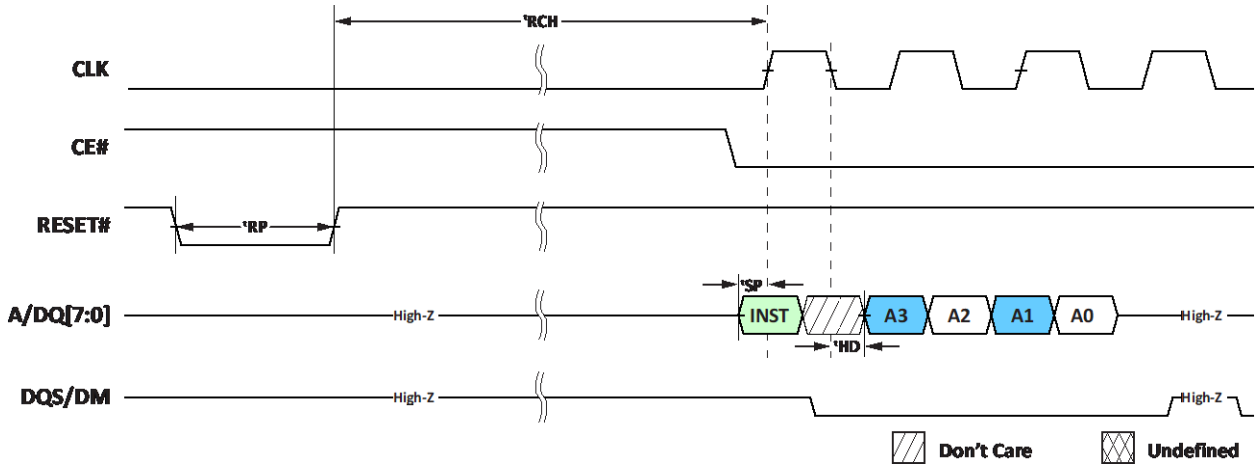


**Figure 15: Deep Power Down Exit with RESET# (Read Operation shown as example)**

Register values are retained in DPD Mode but memory content is not.  However, if a RESET# low is used to exit DPD, register values are also reset to defaults.  tDPDp is minimum period between two DPD Modes (measured from DPD exit to the next DPD entry) as well as from the initial powerup to the first DPD entry.

## 7.9 Halfsleep<sup>TM</sup> Mode

Halfsleep<sup>TM</sup> Mode is a feature which puts the device in an ultra-low power state, while the stored data is retained.  Halfsleep<sup>TM</sup> Mode Entry is entered by writing 8'hF0 into MR6.  CE# going high initiates the Halfsleep<sup>TM</sup> mode and must be maintained for the minimum duration of tHS. The Halfsleep<sup>TM</sup> Entry command sequence is shown below.
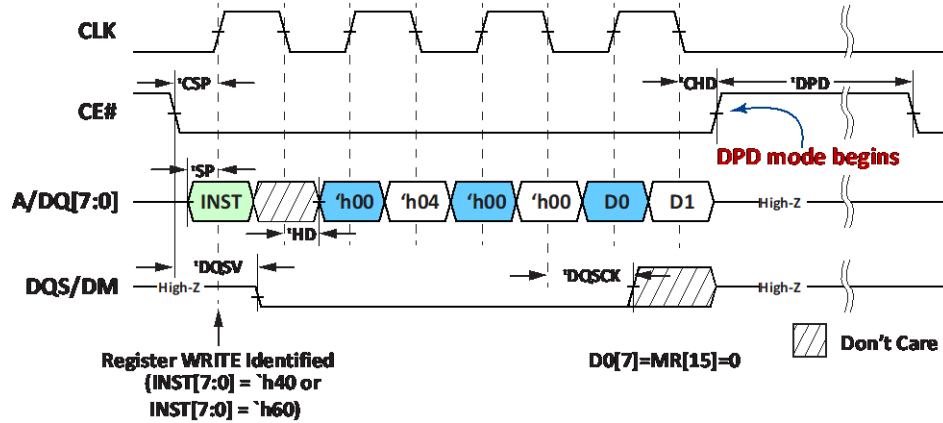


**Figure 16: Halfsleep<sup>TM</sup> Entry**

Halfsleep<sup>TM</sup> Exit is initiated by a low pulsed CE#. Afterwards, CE# should be held high until the first operation begins (observing minimum tXHS).
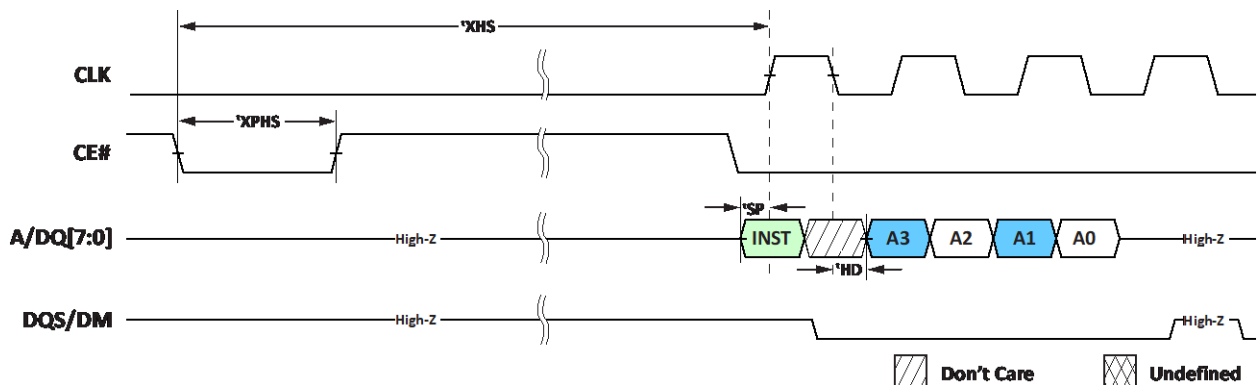


**Figure 17: Halfsleep<sup>TM</sup> Exit**
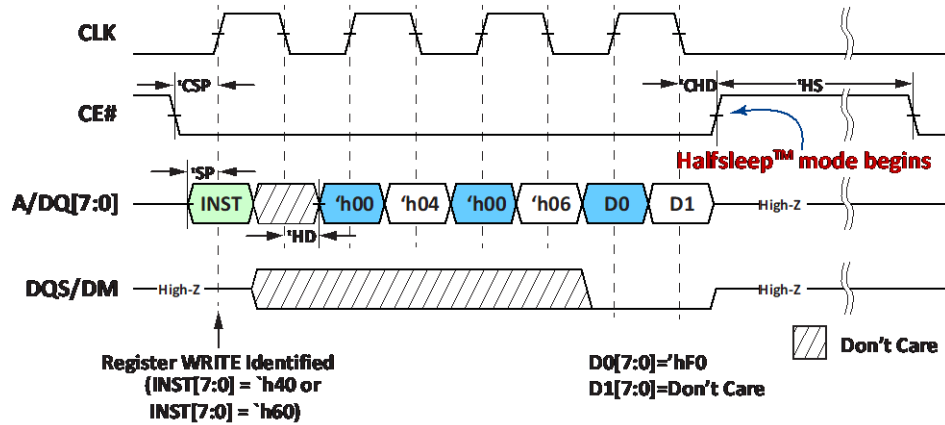
## 8 Electrical Specifications:

### 8.1 Absolute Maximum Ratings

**Table 10: Absolute Maximum Ratings**

| Parameter | Symbol | Rating | Unit | Notes |
|---|---|---|---|---|
| Voltage to any ball except $V_{DD}$, $V_{DDQ}$ relative to $V_{SS}$ | VT | -0.4 to $V_{DD}$/$V_{DDQ}$+0.4 | V | |
| Voltage on $V_{DD}$ supply relative to $V_{SS}$ | $V_{DD}$ | -0.4 to +2.45 | V | |
| Voltage on $V_{DDQ}$ supply relative to $V_{SS}$ | $V_{DDQ}$ | -0.4 to +2.45 | V | |
| Storage Temperature | $T_{STG}$ | -55 to +150 | °C | 1 |

Notes    1:  Storage temperature refers to the case surface temperature on the center/top side of the PSRAM.

Caution:

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification.  Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

### 8.2 Pin Capacitance

**Table 11: Package Pin Capacitance**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input Pin Capacitance | CIN | | 5 | pF | VIN=0V |
| Output Pin Capacitance | COUT | | 6 | pF | VOUT=0V |

Note:  spec'd at 25°C.

**Table 12: Load Capacitance**

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Load Capacitance | $C_L$ | | 15 | pF | |

Note:  System $C_L$ for the use of package.

## 8.3 Decoupling Capacitor Requirement

System designers need to take care of power integrity considering voltage regulator response and the memory peak currents/usage modes.
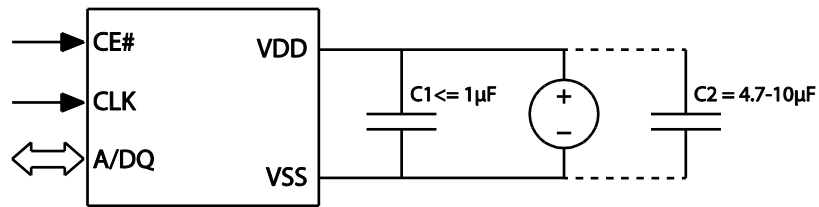


**Figure 18. Decoupling Capacitor**

### 8.3.1 Low ESR cap C1:

It is recommended to place a low ESR decoupling capacitor of <=1µF close to the device to absorb transient peaks.

### 8.3.2 Large cap C2:

During Half-sleep modes even though half-sleep average currents are very small (less than 100µA), device will internally have low duty cycle burst refresh for an extended period of time of a few tens of microseconds. These refresh current peaks are large. During this period if the system regulator cannot supply large peaks for several microseconds, it is important to place a 4.7µF-10µF cap to take care of burst refresh currents and replenish the charge before next burst of refreshes.

If required please contact AP Memory for further current peak details.

## 8.4 Operating Conditions

**Table 13: Operating Characteristics**

| Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|
| Operating Temperature (extended) | -40 | 105 | °C | |
| Operating Temperature (standard) | -40 | 85 | °C | |

## 8.5 DC Characteristics

**Table 14: DC Characteristics**

| Symbol | Parameter | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 1.62 | 1.98 | V | |
| $V_{DDQ}$ | I/O Supply Voltage | 1.62 | 1.98 | V | |
| $V_{IH}$ | Input high voltage | $V_{DDQ}-$ | $V_{DDQ}+0.2$ | V | |
| $V_{IL}$ | Input low voltage | -0.2 | 0.4 | V | |
| $V_{OH}$ | Output high voltage ($I_{OH}$=-0.2mA) | 0.8 | | V | |
| $V_{OL}$ | Output low voltage ($I_{OL}$=+0.2mA) | | 0.2 $V_{DDQ}$ | V | |
| $I_{LI}$ | Input leakage current | | 1 | µA | |
| $I_{LO}$ | Output leakage current | | 1 | µA | |
| $I_{CC}$ | Read/Write @13MHz | | 4 | mA | 1 |
| | Read/Write @133MHz | | 15 | mA | 1 |
| | Read/Write @166MHz | | 20 | mA | 1 |
| | Read/Write @200MHz | | 25 | mA | 1 |
| $ISB_{EXT}$ | Standby current (105C) | | 1100 | µA | 2 |
| $ISB_{STD}$ | Standby current (85C) | | 680 | µA | 2 |
| $ISB_{STDDPD}$ | Standby current (Deep Power Down -40°C to 85°C) | | 20 | µA | 7 |

Note    1: Current is only characterized.

Note    2: Without CLK toggling.  ISB will be higher if CLK is toggling.

Note    3: 0.5x Refresh.

Note    4: **Typical mean $ISB_{STDROOM}$ 100uA**.

Note    5: Current is only guaranteed after 150ms into Halfsleep™ mode.

Note    6: **Typical mean $ISB_{STDHS}$ 40uA**

Note    7: **Typical mean $ISB_{STDDPD}$ 8uA at 25˚C**

## 8.6 AC Characteristics

**Table 11: READ/WRITE Timing**

| Symbol | Parameter | -7(133MHz) Min | -7(133MHz) Max | -6(166MHz) Min | -6(166MHz) Max | -5(200MHz) Min | -5(200MHz) Max | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| tCLK | CLK period | 7.5 | | 6 | | 5 | | ns | |
| tCH/tCL | Clock high/low width | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | tCLK | |
| tKHKL | CLK rise or fall time | | 1.2 | | 1 | | 0.8 | ns | |
| tCEM | CE# low pulse width | | 4 | | 4 | | 4 | µs | Standard |
| | | | 1 | | 1 | | 1 | µs | Extended |
| tCEM | CE# low pulse width | 3 | | 3 | | 3 | | tCLK | Minimum 3 |
| tCPH | CE# high pulse width | 15 | | 18 | | 20 | | ns | Clocking |
| tCSP | CE# setup time to CLK rising edge | 2 | | 2 | | 2 | | ns | |
| tCHD | CE# hold time from CLK falling | 2 | | 2 | | 2 | | ns | |
| tSP | Setup time to active CLK edge | 0.8 | | 0.6 | | 0.5 | | ns | |
| tHD | Hold time from active CLK edge | 0.8 | | 0.6 | | 0.5 | | ns | |
| tDQSV | Chip enable to DQS output low | 2 | 6 | 2 | 6 | 2 | 6 | ns | |
| tHZ | Chip disable to DQ/DQS output | | 6 | | 6 | | 6 | ns | |
| tRC | Write Cycle | 60 | | 60 | | 60 | | ns | |
| tRC | Read Cycle | 60 | | 60 | | 60 | | ns | |
| tHS | Minimum Halfsleep$^{TM}$ duration | 150 | | 150 | | 150 | | µs | |
| tXHS | Halfsleep$^{TM}$ Exit CE# low to CLK setup time | 150 | | 150 | | 150 | | µs | |
| tXPHS | Halfsleep$^{TM}$ Exit CE# low pulse width | 60 | | 60 | | 60 | | ns | |
| | | | tCEM | | tCEM | | tCEM | µs | Standard |
| | | | | | | | | µs | Extended |
| tDPD | Minimum DPD Duration | 500 | | 500 | | 500 | | µs | |
| tDPDp | Minimum period between DPD | 500 | | 500 | | 500 | | µs | |
| tXDPD | DPD CE# low to CLK setup time | 150 | | 150 | | 150 | | µs | |
| tXPDPD | DPD Exit CE# low pulse width | 60 | | 60 | | 60 | | ns | |
| | | | 2 | | 2 | | 2 | µs | |
| tPU | Device Initialization | 150 | | 150 | | 150 | | µs | |
| tCHR | Chip-disable to RESET# low | 20 | | 20 | | 20 | | ns | |
| tRP | RESET# low pulse width | 1 | | 1 | | 1 | | µs | |
| tRST | Reset to CMD valid | 2 | | 2 | | 2 | | µs | |
| tRCH | RESET# to CMD valid | 150 | | 150 | | 150 | | µs | |

**Table 12: DDR timing parameters**

| Symbol | Parameter | -7(133MHz) | | -6(166MHz) | | -5(200MHz) | | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | | |
| tCQLZ | Clock rising edge to DQS low | 1 | 6 | 1 | 6 | 1 | 6 | ns | |
| tDQSCK | DQS output access time from CLK | 2 | 5.5 | 2 | 5.5 | 2 | 5.5 | ns | |
| tDQSQ | DQS – DQ skew | | 0.6 | | 0.5 | | 0.4 | ns | |
| tDS | DQ and DM input setup time | 0.8 | | 0.6 | | 0.5 | | ns | |
| tDH | DQ and DM input hold time | 0.8 | | 0.6 | | 0.5 | | ns | |

## 9 Change Log

| Version | Who | Date | Description |
|---|---|---|---|
| 0.01 | | Apr. 03, 2019 | Initial version derived from E3 1.61 |
| 0.02 | | Jul. 08, 2019 | Update Table 3 ,7, 9, DC characteristics. Add Halfsleep$^{TM}$ mode. |
| 0.03 | | Jul. 15, 2019 | Update Figure 3, 16, 17, and 19 |
| 0.04 | | Jul. 16, 2019 | Update part number, command truth table, Figure 1, Table 12, 16, ball assignment |
| 0.05 | | Jul. 17, 2019 | Update VDDQ information |
| 0.06 | | Jul. 17, 2019 | Update bare die pin capacitance |
| 0.07 | | Aug 23, 2019 | Updated tHS, tXPDPD, Wrap & hybrid burst, package code |
| 0.08 | | Oct 18, 2021 | tCEM revised data by BD suggest (E7_OPI_256Mb/512Mb)<br>Standard temp: 2 us -> 4 us.<br>Extended temp: 0.5 us -> 1 us. |
| 1.0 | Kim | Sep 02, 2022 | Revised typos |