DOUBLE-DATA-RATE QPI PSRAM

Specifications

- Single Supply Voltage:
  - V_{DD}=1.62 to 1.98V
- Interface: QPI (quad peripheral interface)
- Performance:
  Clock rate up to 166MHzs
- Organization: 16Mb, 2M x 8bits
- Addressable bit range: A[20:0]
  (array accesses must start on EVEN addresses only, e.g., A[0]=0)
- Page Size: 512 bytes
- Refresh: Self-managed
- Operating temperature range
  - Tc = -40°C to +85°C (standard range)
  - Tc = -40°C to +105°C (extended range)
- Maximum Standby Current:
  - 150µA @ 105°C
  - 100µA @ 85°C
- Typical Standby Current:
  - 20µA @ 25°C

Features

- 100 & 200Ω Configurable Output Drive Strength LVCMOS.
- Register configurable wrap lengths of 16,32,64 and 512.
- Software reset.

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1 Table of Contents

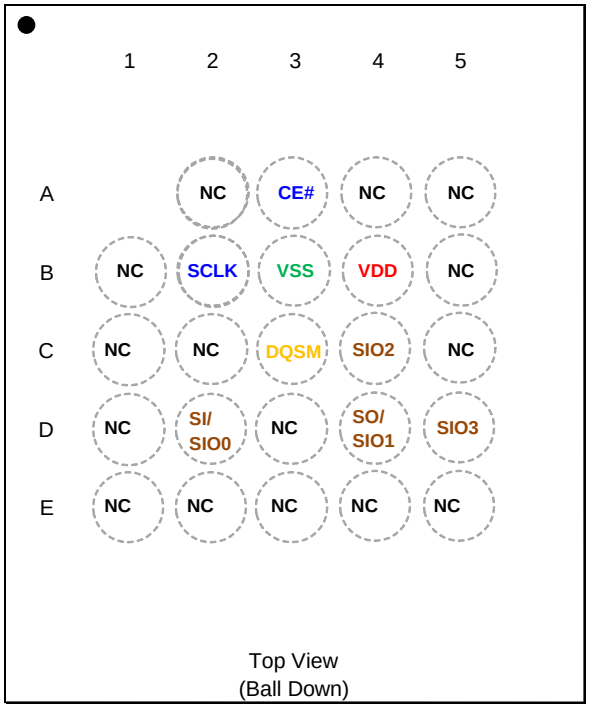
2 Introduction

This Pseudo-SRAM device features a high speed, low pin count interface. It has 4 DDR I/O pins and operates in QPI (quad peripheral interface) mode with frequencies up to 166 MHz. The data input (A/DQ) to the memory relies on clock (CLK) to latch all instructions, addresses and data. It is most suitable for low-power and low cost portable applications. It incorporates a seamless self-managed refresh mechanism. Hence it does not require the support of DRAM refresh from system host. The self-refresh feature is a special design to maximize performance of memory read operation.

3 Package Information

The APS1604M-DQxRA is available in mini-BGA 24B package 6 x 8 x 1.2mm, ball pitch 1.0mm,ball size 0.4mm package code(BA) .

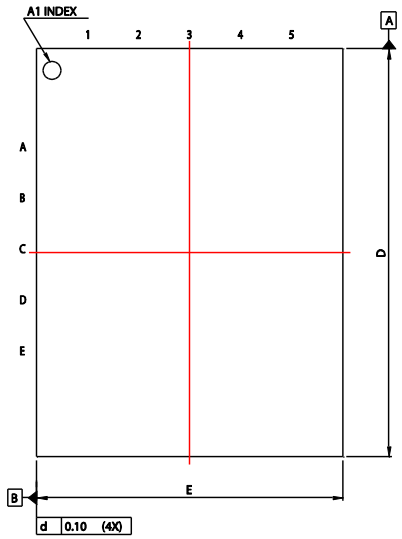
- Ball Assignment for MINI-BGA 24B



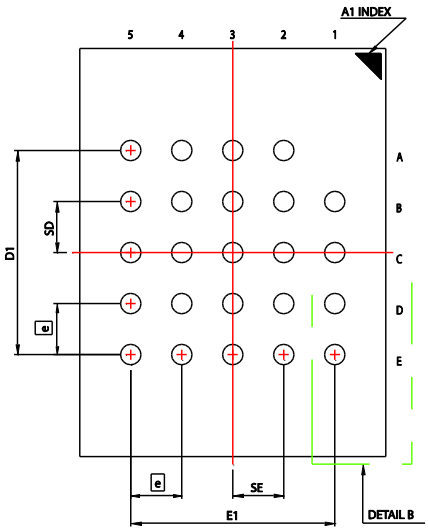
(6x8x1.2mm)(P1.0)(B0.4)

4 Package Outline Drawing

TOP VIEW

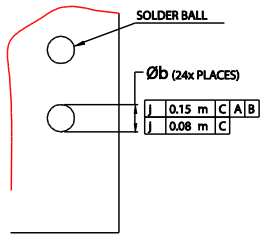


BOTTOM VIEW

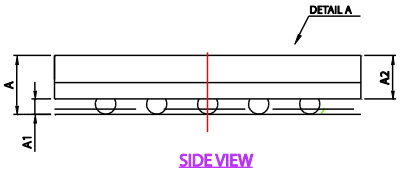


SYM.	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.25	0.30	0.35
A2	-	0.79	-
b	0.35	0.40	0.45
D	7.90	8.00	8.10
D1	4.00 BSC		
E	5.90	6.00	6.10
E1	4.00 BSC		
SE	1.00 TYP		
SD	1.00 TYP		
e	1.00 BSC		

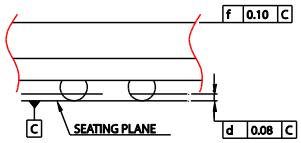
NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.
3. THE DIAMETER OF PRE-REFLOW SOLDER BALL IS Ø0.40mm.(0.35mm SMO)



DETAIL B



SIDE VIEW

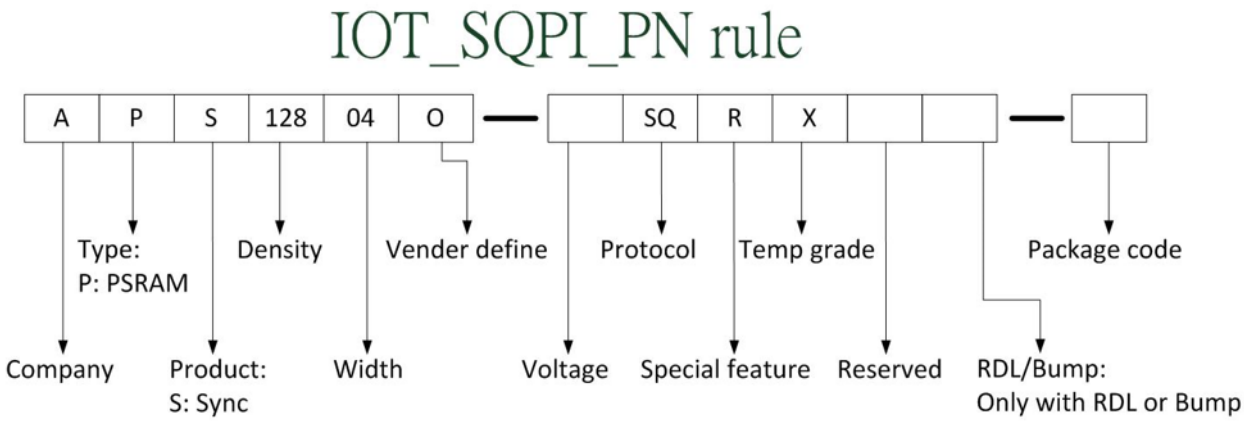


DETAIL A

5 Ordering Information

Table 1: Ordering Information

Part Number	*Temperature Range*	*Max Frequency*	*Note*
APS1604M-DQRA	Tj=-40°C to +85°C	166 MHz	Bare die, SIP
APS1604M-DQXRA	Tj=-40°C to +105°C	166 MHz	Bare die, SIP
APS1604M-DQRA-BA	Tc=-40°C to +85°C	166 MHz	BGA 24B (Only for validation)



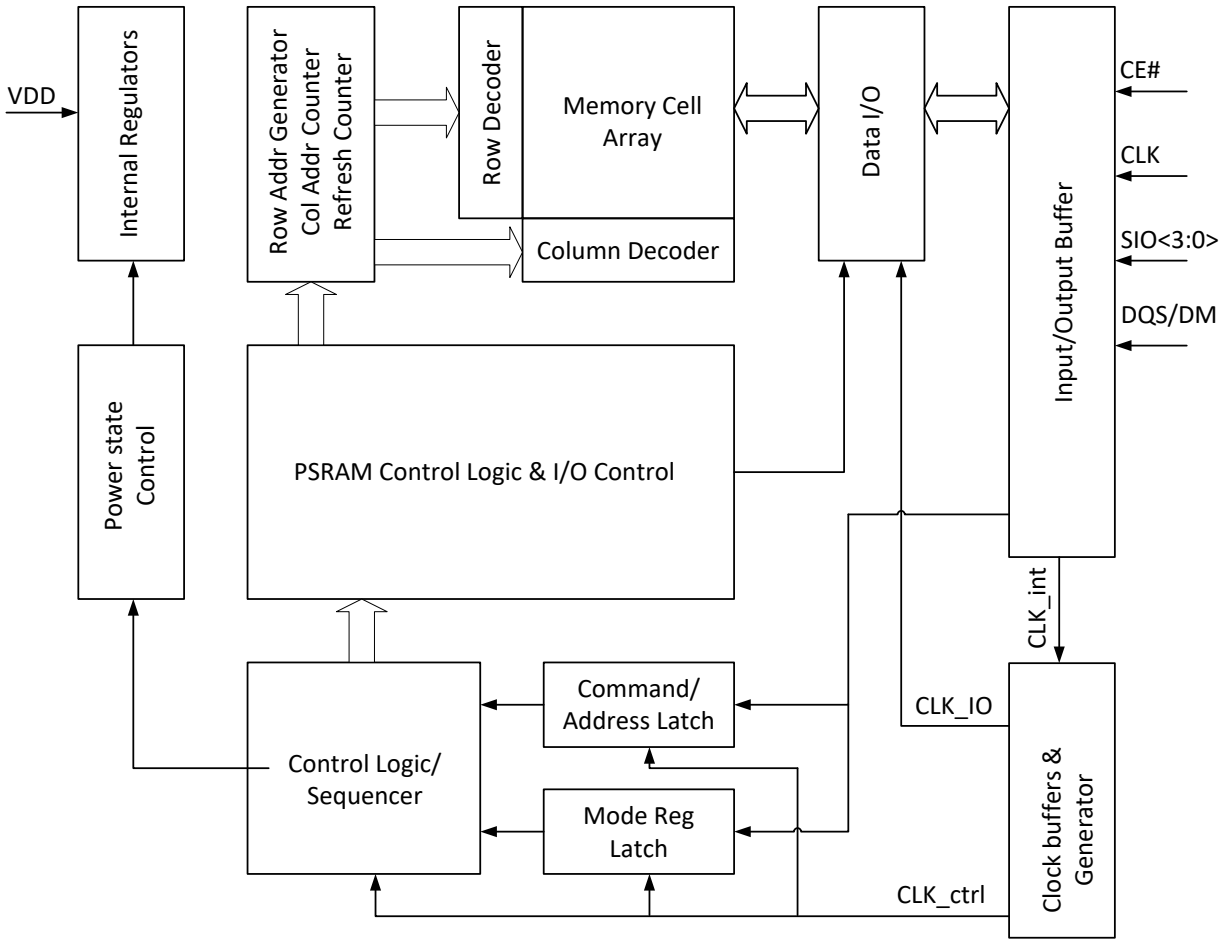
6 Signal Table

All signals are listed in Table 2.

Table 2: Signals Table

Symbol	*Type*	*QPI Mode Function*	*Comments*
V_{DD}	Power	Core supply 1.8V	
VSS	Ground	Core supply ground	
CE#	Input	Chip select, active low. When CE#=1, chip is in standby state	
CLK	Input	Clock Signal	
SIO[0]	IO	IO[0]	
SIO[1]	IO	IO[1]	
SIO[2]	IO	IO[2]	
SIO[3]	IO	IO[3]	
DQS/DM	IO	Data mask during memory writes, DQS during memory reads	

7 Block diagram



8 Power-Up Initialization

QPI products include an on-chip voltage sensor used to start the self-initialization process. When V_{DD} reaches a stable level at or above minimum V_{DD}, the device will take up to 150µs to complete initialization. It also requires host to issue RESET Operation (see section 13) before any memory/register access. From the beginning of power ramp to the end of the 150µs period, CLK should remain LOW, CE# should remain HIGH (track V_{DD} within 200mV) and SIO[3:0] should remain LOW.

After the Device Reset tRST≧50ns period the device is ready for normal operation.

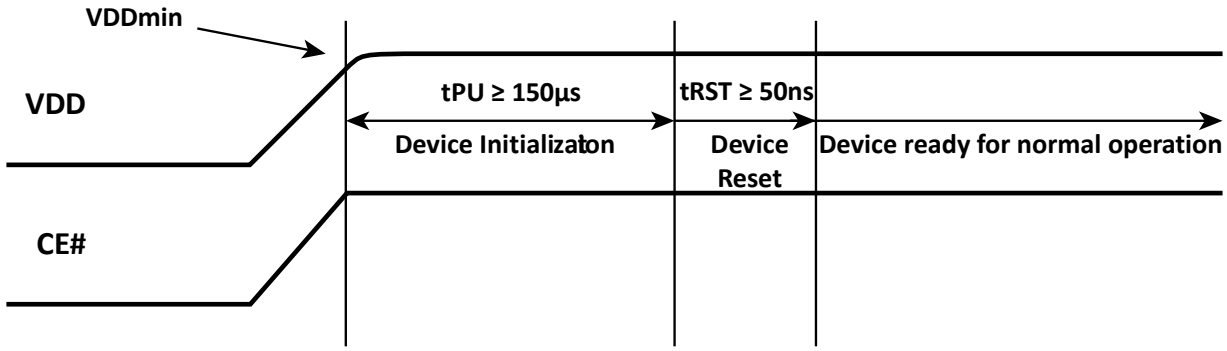


Figure 1. Power-Up Initialization Timing

9 Interface Description

9.1 Address Space

DDR QPI PSRAM device is byte-addressable. 16M device is addressed with A[20:0].

9.2 Page Length

Read and write operations have a page size of 512 bytes.

9.3 Drive Strength

The device powers up in 200Ω.

9.4 Power-on Status

The device powers up in DDR QPI Mode. It is required to have CE# high before beginning any operations.

10 Mode Register Definition

Table 3: Mode Register Table

MR No.	MA[3:0]	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	`h0	R/W	rsvd.	Wrap		Latency			DQ Zout	

Table 4: Wrap Codes MR0[6:5]

Wrap Burst Settings	
MR0[6:5]	Wrapped Length
00	16
01	32
10	64
11 (default)	512 (page size)

Table 5: Latency Configuration Codes MR0[4:2]

Latency Codes (LC)			Max Input CLK Freq (MHz)	
MR0[4:2]	Write Latency (LC)	Read Latency (LC+1)	Standard	Extended
010	2	3	84	84
011	3	4	104	104
100 (default)	4	5	133	133
101	5	6	166	166
others	reserved	-	-	-

Table 6: DQ Output Drive Strength Codes MR0[1:0]

DQ Output Drive Strength	
MR0[1:0]	Impedance
01	100Ω
10 (default)	200Ω
others	reserved

11 Command/Address Latching Truth Table

The device recognizes the following commands.

Command	*Code*	*Cmd*	*Addr*	*Wait Cycle*	*DIO*	*Max Freq.*
Wrapped Read	'h8B	Q	Q	LC+1	Q	166
Wrapped Write	'h82	Q	Q	LC	Q	166
Mode Register Read	'hB5	Q	Q	LC+1	Q	166
Mode Register Write	'hB1	Q	Q	0	Q	166
Reset Enable	'h66	Q	-	-	-	166
Reset	'h99	Q	-	-	-	166

Remark: Q = Quad IO; Command cycles are SDR, Address and Data cycles are DDR.

11.1 Command Termination

All Reads & Writes must be completed by raising CE# high immediately afterwards in order to terminate the active read/write wordline and set the device into standby. Not doing so will block internal refresh operations and cause memory failure. For write operations sufficient ^{t}CHD will ensure final write data is latched and written, while ^{t}CSP2 ensures no extra writes occurs once CE is HIGH.

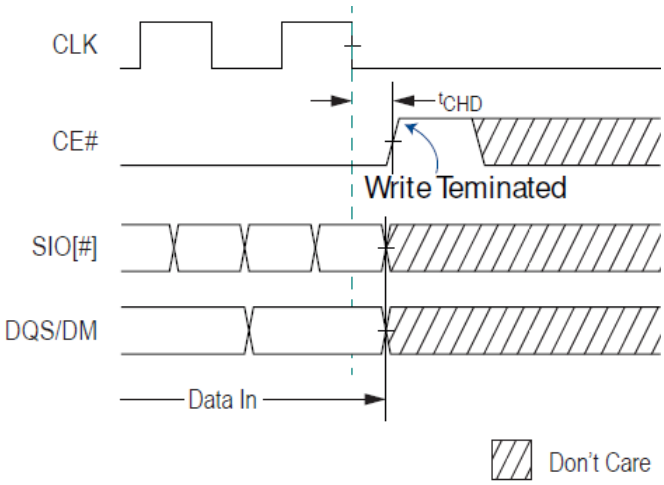


Figure 2**: Write Command Termination (no CLK during CE high)**

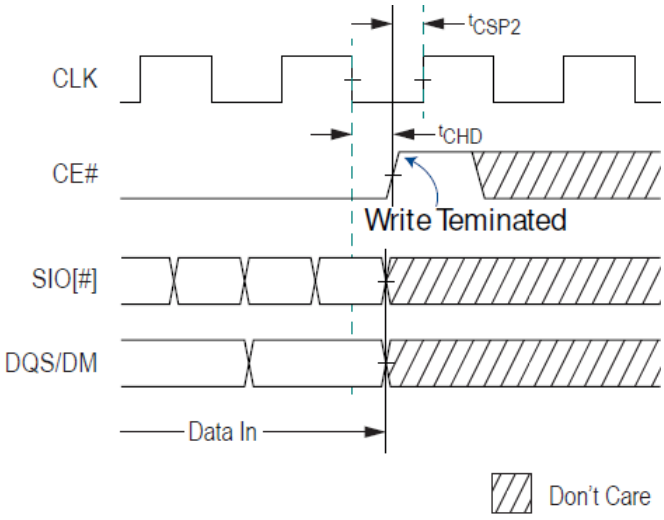


Figure 3: Write Command Termination (CLK during CE high)

For a memory controller to correctly latch the last piece of data prior to read termination, it is recommended to provide a longer CE# hold time (^{t}CHD +^{t}HZ> ^{t}DQSCK) for a sufficient data window.

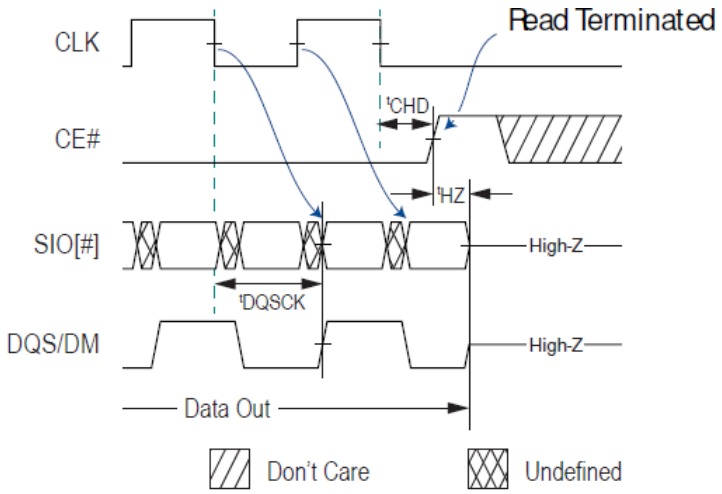


Figure 4: Read Command Termination

12 Mode Register Operations

12.1 QPI MR Read Operation

For all reads, MR data will be available ^{t}DQSCK after the falling edge of CLK.

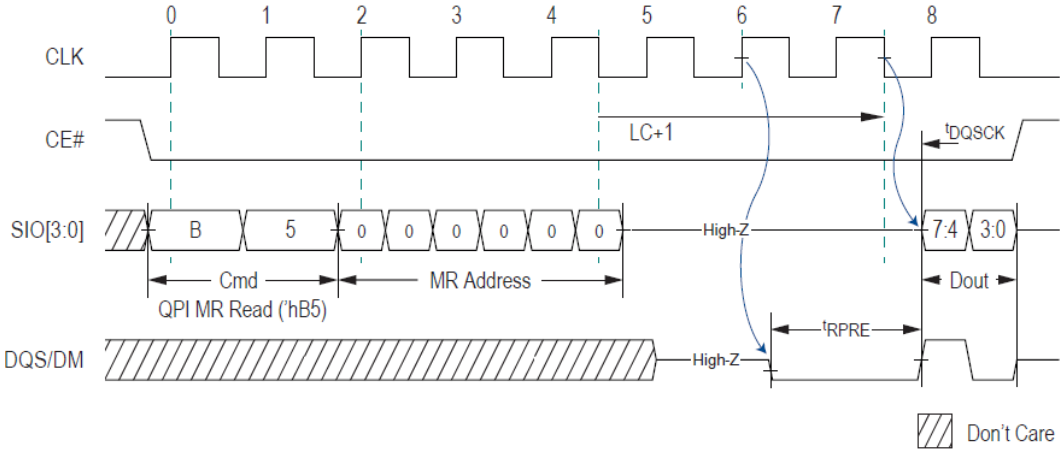


Figure 5: QPI MR Read 'hB5 (Latency Code 2 shown)

12.2 QPI MR Write Operation

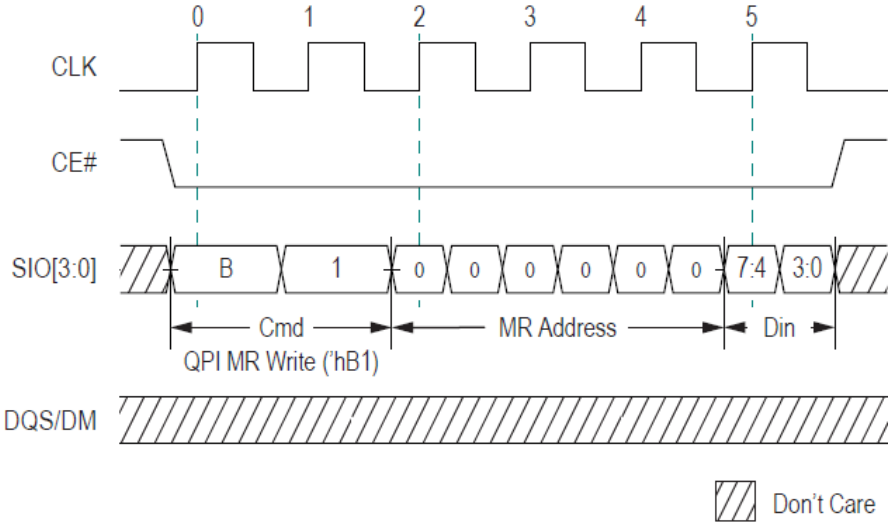


Figure 6: QPI MR Write 'hB1

13 Memory Operations

Write and read operations must start on even addresses (e.g., A[0]=0) only. Minimum read or write length is 1 byte.

13.1 QPI Read Operations

For all reads, data will be available ^{t}DQSCK after the falling edge of CLK.

QPI Reads can be done by issuing the command 'h8B.

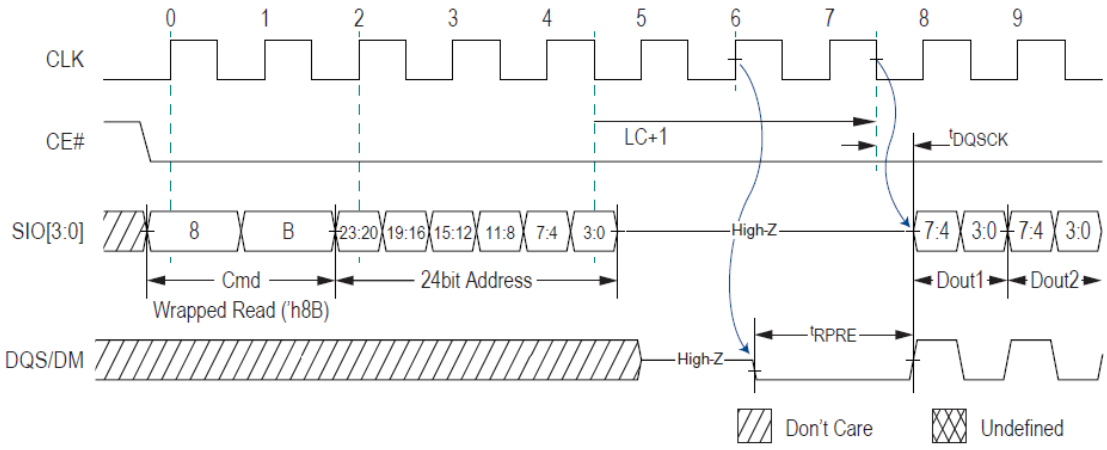


Figure 7: QPI Fast Quad Read 'h8B (Latency Code 2 shown)

13.2 QPI Write Operation(s)

QPI Writes can be done by issuing the command 'h82:

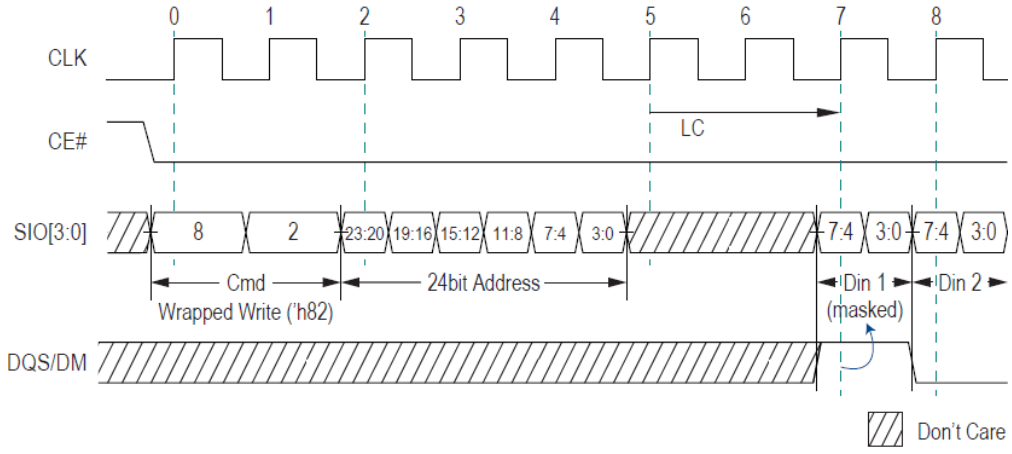


Figure 8: QPI Write 'h82 (Latency Code 2 shown)

14 Reset Operation

The Reset operation is used to puts the device back to its default mode after power-up. This is a 2-step operation which consists of two commands: Reset-Enable (RSTEN) and Reset(RST).

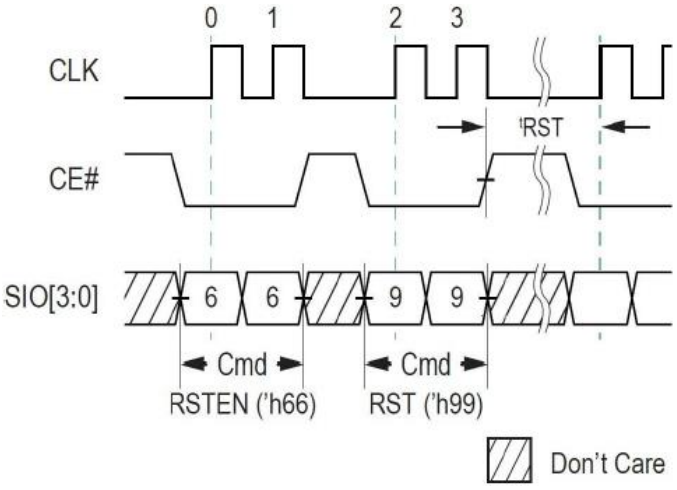


Figure 9: QPI Reset

Reset command has to immediately follow the Reset-Enable command in order for reset operation to take effect. Any command other than the Reset command after the Reset-Enable command will cause the device to exit Reset-Enable state and abandon reset operation.

15 Input/Output Timing

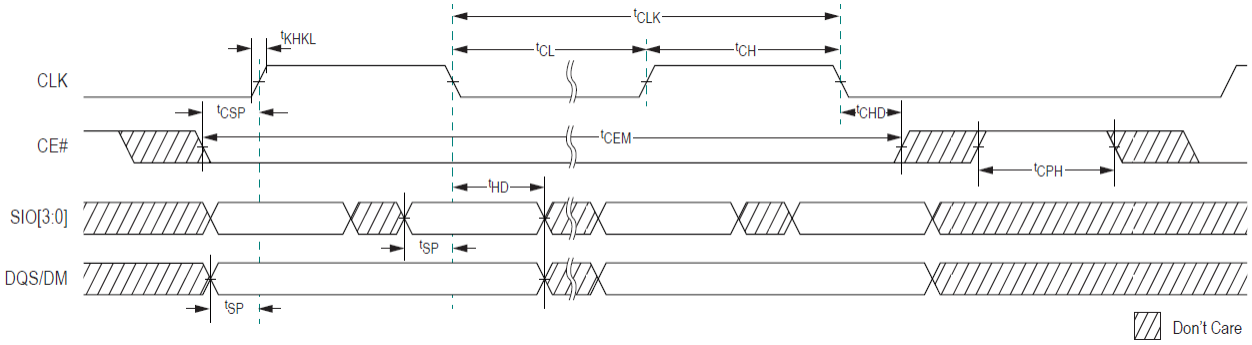


Figure 10: Input Timing

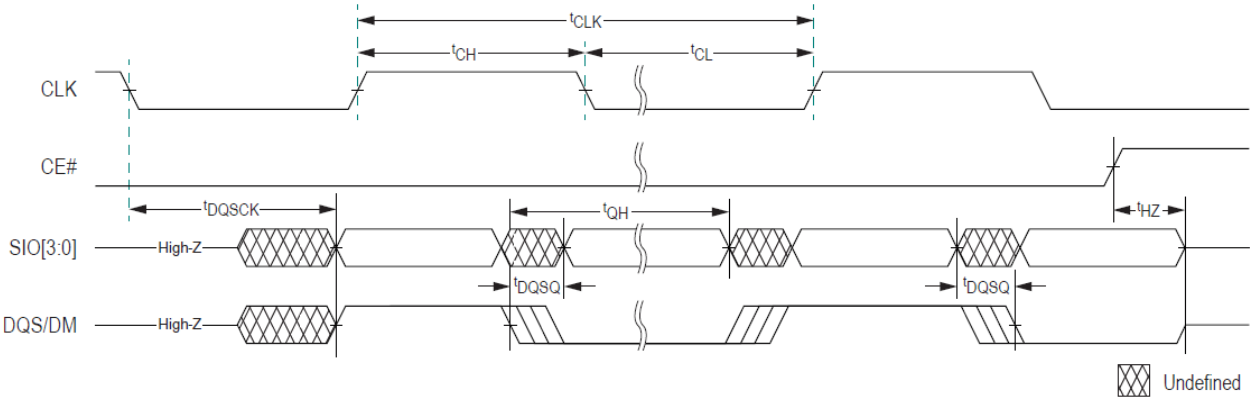


Figure 11: Output Timing

16 Electrical Specifications:

16.1 Absolute Maximum Ratings

Table 7: Absolute Maximum Ratings

Parameter	*Symbol*	*Rating*	*Unit*	*Notes*
Voltage to any ball except V_{DD} relative to V_{SS}	VT	-0.3 to V_{DD}+0.3	V	
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.2 to +2.45	V	
Storage Temperature	T_{STG}	-55 to +150	°C	1

Notes 1: Storage temperature refers to the case surface temperature on the center/top side of the PSRAM.

Caution:
Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

16.2 Pin Capacitance

Table 8: Package Pin Capacitance

Parameter	*Symbol*	*Min*	*Max*	*Unit*	*Notes*
Input Pin Capacitance	CIN		6	pF	VIN=0V
Output Pin Capacitance	COUT		8	pF	VOUT=0V

Note: spec'd at 25°C.

Table 9: Bare Die Pin Capacitance

Parameter	*Symbol*	*Min*	*Max*	*Unit*	*Notes*
Input Pin Capacitance	CIN		2	pF	VIN=0V
Output Pin Capacitance	COUT		3	pF	VOUT=0V

Note: spec'd at 25°C.

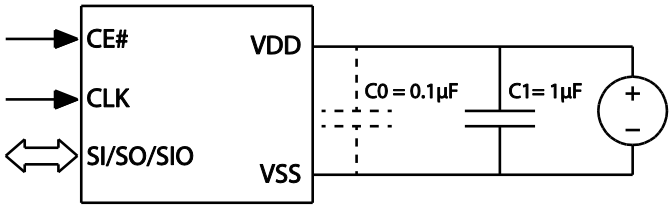
Table 10: Load Capacitance

Parameter	*Symbol*	*Min*	*Max*	*Unit*	*Notes*
Load Capacitance	C_L		15	pF	

Note: System C_L for the use of package

16.3 Decoupling Capacitor Requirement

It is required to have a decoupling capacitor on VDD pin for IO switchings and psram internal transient events. A low ESR 1µF ceramic cap is recommended. To minimize parasitic inductance, place the cap as close to VDD pin as possible. An optional 0.1uF can further improve high frequency transient response.



Note 1: that the length of grounding connection between PSRAM and PCB must be as short as possible. Having ground plane on PCB and multipoint ground would be preferred (to avoid single-point grounding topology).The width of VDD and VSS traces would be suggested more than 20mil.

16.4 Operating Conditions

Table 11: Operating Characteristics

Parameter	*Min*	*Max*	*Unit*	*Notes*
Operating Temperature (extended)	-40	105	°C	
Operating Temperature (standard)	-40	85	°C	

16.5 DC Characteristics

Table 12: DC Characteristics

Symbol	*Parameter*	*Min*	*Max*	*Unit*	*Notes*
V_{DD}	Supply Voltage	1.62	1.98	V	
V_{IH}	Input high voltage	V_{DD}-0.4	V_{DD}+0.2	V	
V_{IL}	Input low voltage	-0.2	0.4	V	
V_{OH}	Output high voltage (I_{OH}=-0.2mA)	0.8 V_{DD}		V	
V_{OL}	Output low voltage (I_{OL}=+0.2mA)		0.2 V_{DD}	V	
I_{LI}	Input leakage current		1	µA	
I_{LO}	Output leakage current		1	µA	
I_{CC}	Read/Write		15	mA	1
ISB_{EXT}	Standby current (105C)		150	µA	2
ISB_{STD}	Standby current (85C)		100	µA	2

Note 1: Output load current not included.

2: Standby current is measured when CLK is in DC low state.

16.6 AC Characteristics

Table 13: READ/WRITE Timing

Symbol	*Parameter*	*Min*	*Max*	*Unit*	*Notes*
^{t}CLK	CLK period SIP	6		ns	166MHz*
^{t}CH/^{t}CL	Clock high/low width	0.45	0.55	^{t}CLK(min	
^{t}KHKL	CLK rise or fall time		0.8	ns	1
^{t}CPH	CE# HIGH between subsequent burst operations	20		ns	
^{t}CEM	CE# low pulse width		3	µs	Extended grade
			8		Standard grade
^{t}CSP	CE# setup time to CLK rising edge (CE# low)	2		ns	
^{t}CSP2	CE# setup time to CLK rising edge (CE# high)	1		ns	
^{t}CHD	CE# hold time from CLK falling edge SIP	0.5		ns	
	CE# hold time from CLK falling edge PKG	0.5		ns	
^{t}SP	Setup time to active CLK edge	0.8		ns	
^{t}HD	Hold time from active CLK edge	0.8		ns	
^{t}RPRE	DQS read preamble	1.5		^{t}CLK	
^{t}HZ	Chip disable to DQ output high-Z	0	6	ns	
^{t}DQSCK	DQS output access time from CLK	2	5.5	ns	1
^{t}DQSQ	DQS – DQ skew		0.5	ns	
^{t}RST	Time between end of RST CMD to next valid CMD	50		ns	

Note

1: Measured from 20% to 80% V_{DD}.

17 Change Log

Version	Who	Date	Description
1.0		Jul 31, 2020	Initial Version
1.1		Oct 13, 2020	Remove all room temperature maximum spec.
1.2		Oct 26, 2021	Revised tCEM value from 4us to 3us @105C
1.3		Dec 03, 2021	Added a description "array accesses must start on EVEN addresses only Revised Ordering Information and naming rule table
1.3a		Jan 03, 2022	Revised typo caused by version 1.2 to 1.3 **Addressable Bit Range:** A[23:0] to A[20:0] .
1.3b	Alan	Jan 25, 2022	Revise part description from DQRAx to DQXRA
1.4	Kim/ Gene/ Eric	Jun 16, 2022	Typos correct