Double-Data-Rate Octal SPI PSRAM

Specifications

- **Single Supply Voltage**
  - VDD=1.62 to 1.98V
  - VDDQ=1.62 to 1.98V
- **Interface**: Octal SPI with DDR mode, two bytes transfers per one clock cycle
- **Performance**: Clock rate up to 200MHz, 400MB/s read/write throughput
- **Organization**: 64Mb, 8M x 8bits with 1024 bytes page size
  - Column address: AY0 to AY9
  - Row address: AX0 to AX12
- **Refresh**: Self-managed
- **Operating Temperature Range**
  - T_{OPER} = -40°C to +85°C(standard range)
  - T_{OPER}= -40°C to +105°C (extended range)
- **Maximum Standby Current**
  - 300µA @ 105°C
  - 200µA @ 85°C
- **Typical Standby Current:**
  - 20µA @ 25°C (Halfsleep™ Mode with data retained)

Features

- **Low Power Features**
  - Partial Array Self-Refresh (PASR)
  - Auto Temperature Compensated Self-Refresh (ATCSR) by built-in temperature sensor
  - User configurable refresh rate
  - Ultra Low Power (ULP) Halfsleep™ mode with data retained
- **Software Reset**
- **Reset Pin Available**
- **Output driver LVCMOS** with programmable drive strength
- **Data Mask (DM)** for write data
- **Data Strobe (DQS)** enabled highspeed read operation
- **Register Configurable** write and read initial latencies
- **Write Burst Length**, maximum 1024 bytes, minimum 2 bytes.
- **Wrap** & **Hybrid Burst** in 16/32/64/1K lengths.
- **Linear Burst Command**
- **Row Boundary Crossing (RBX)**
  - read operations can be enabled via Mode Register.
  - RBX Write is NOT supported.

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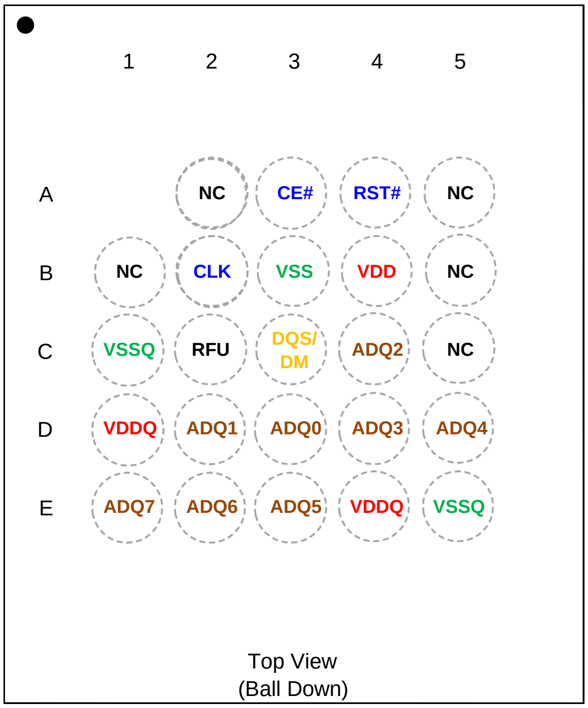
2 Package Information

The APS6408L-OBMx is available in mini-BGA 24B package 6 x 8 x 1.2mm, ball pitch 1.0mm,ball size 0.4mm , package code "BA".

- Ball Assignment for MINI-BGA 24B



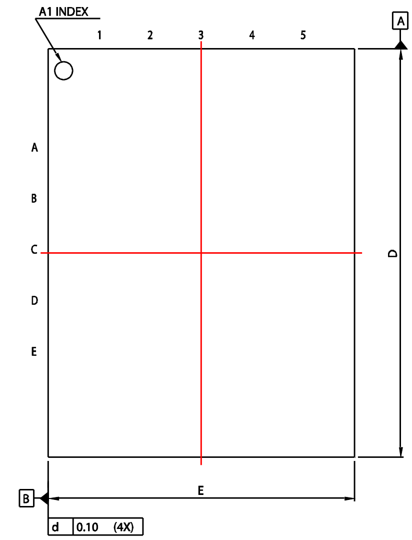
(6x8x1.2mm)(P1.0)(B0.4)

Note:

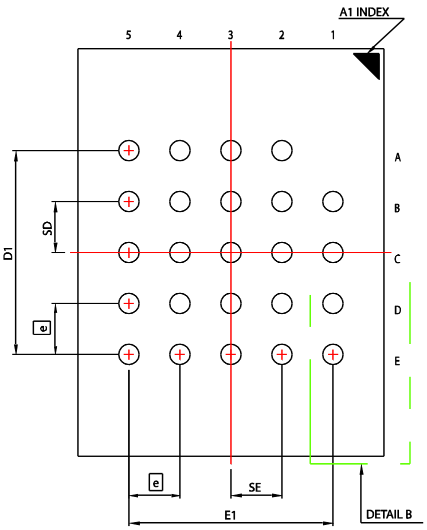
1. Part Number APS6408L-OBM-BA for 64Mb.
2. RFU: Reserved for future use, which is reserved for 2nd CE#.
3. NC: No internal connection.

3 Package Outline Drawing

TOP VIEW

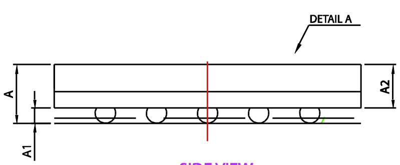


BOTTOM VIEW

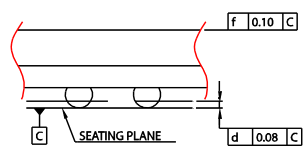


SYM.	DIMENSION (mm)		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.25	0.30	0.35
A2	-	0.79	-
b	0.35	0.40	0.45
D	7.90	8.00	8.10
D1	4.00 BSC		
E	5.90	6.00	6.10
E1	4.00 BSC		
SE	1.00 TYP		
SD	1.00 TYP		
e	1.00 BSC		

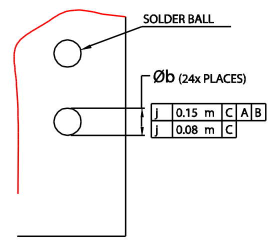
NOTE:
1. CONTROLLING DIMENSION : MILLIMETER.
2. REFERENCE DOCUMENT : JEDEC MO-207.
3. THE DIAMETER OF PRE-REFLOW SOLDER BALL IS Ø0.40mm.(0.35mm SMO)



SIDE VIEW



DETAIL A



DETAIL B

4 Ordering Information

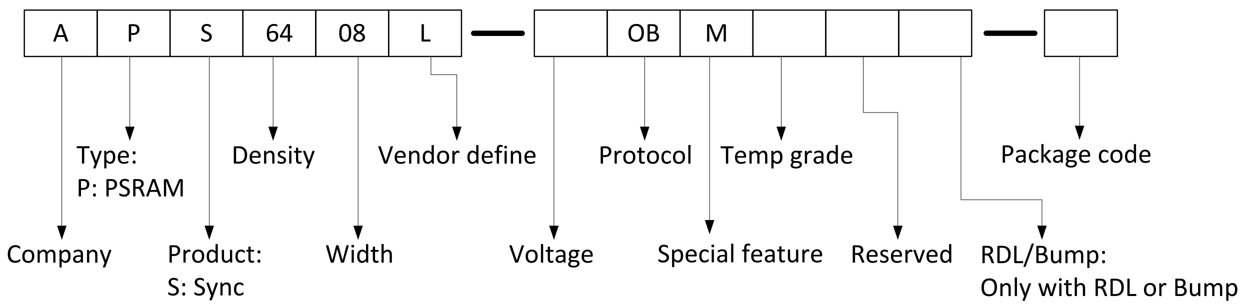
Table 1: Ordering Information

Part Number	Temperature Range	Max Frequency	Note
APS6408L-OBM	Tj= -40°C to +85°C	200 MHz	Bare die, SIP
APS6408L-OBMX	Tj= -40°C to +105°C	200 MHz	Bare die, SIP
APS6408L-OBM-BA	Tc= -40°C to +85°C	200 MHz	BGA 24B
APS6408L-OBMX-BA	Tc= -40°C to +105°C	200 MHz	BGA 24B

Note

- OBM is standard part to support RBX read operation only.

IOT_SOPI_PN rule



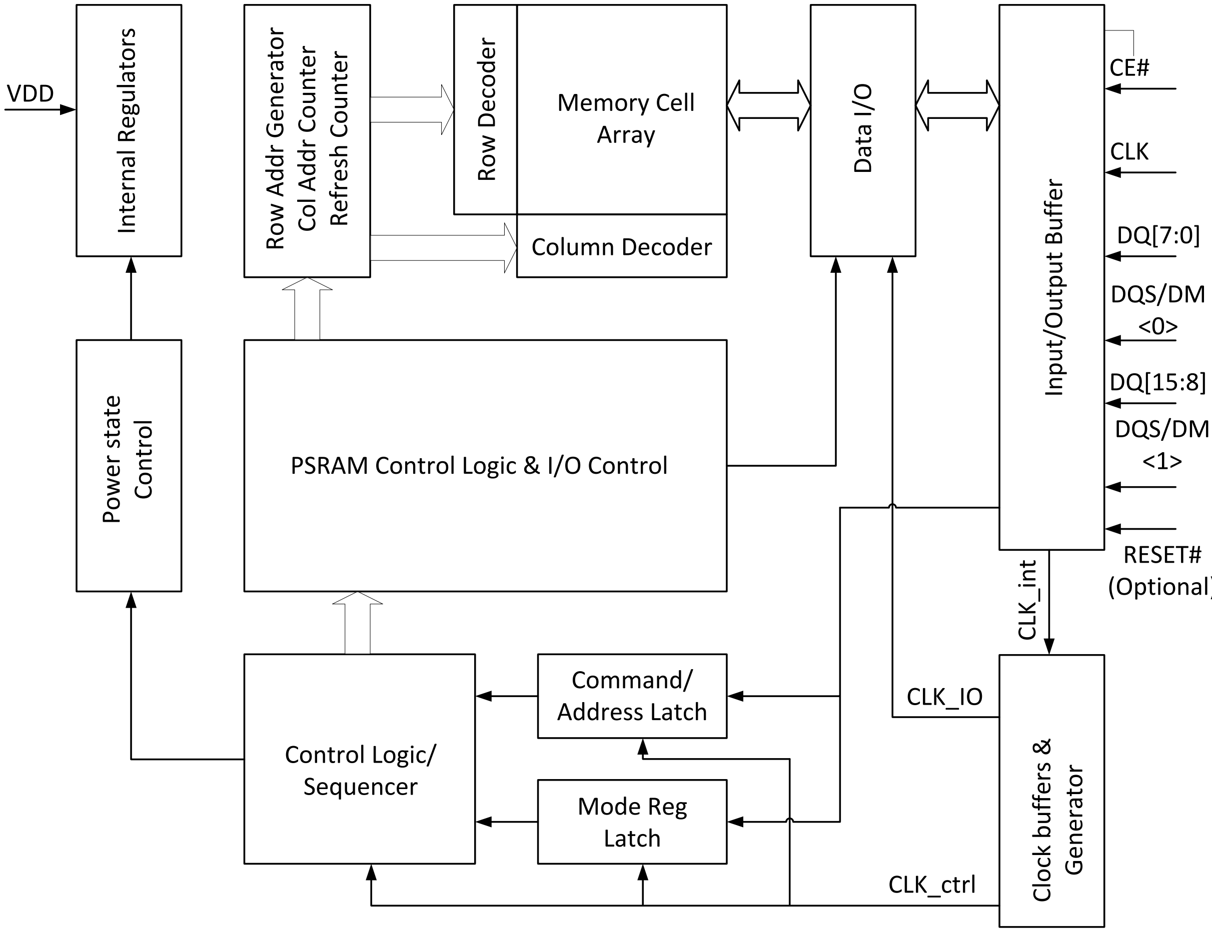
5 Signal Table

All signals are listed in Table 2.

Table 2: Signals Table

Symbol	*Type*	*Description*	*Comments*
V_{DD}	Power	Core supply 1.8V	
V_{DDQ}	Power	IO supply 1.8V	
V_{SS}	Ground	Core supply ground	
V_{SSQ}	Ground	IO supply ground	
A/DQ[7:0]	IO	Address/DQ bus [7:0]	
DQS/DM	IO	DQ strobe clock during reads, Data mask during writes. DM is active high. DM=1 means "do not write".	
CE#	Input	Chip select, active low. When CE#=1, chip is in standby state.	
CLK	Input	Clock signal	
RESET#	Input	Reset signal, active low. Optional, as the pad is internally tied to a weak pull-up and can be left floating.	

6 Block diagram



7 Power-Up Initialization

Octal DDR products include an on-chip voltage sensor used to start the self-initialization process. V_{DD} and V_{DDQ} must be applied simultaneously. When they reach a stable level at or above minimum V_{DD}, the device is in Phase 1 and will require 150µs to complete its self-initialization process. The user can then proceed to Phase 2 of the initialization described in this section.

During Phase 1 CE# should remain HIGH (track V_{DD} within 200mV); CLK should remain LOW.

After Phase 2 is complete the device is ready for operation, however Halfsleep™ entry and Deep Power Down (DPD) entry are not available until Halfsleep™ Power Up (tHSPU) or DPD Power Up (tDPDp) duration is observed.

7.1 Power-Up Initialization Method 1 (via. RESET# pin)

The RESET# pin can be used to initialize the device during Phase 2 as follows:

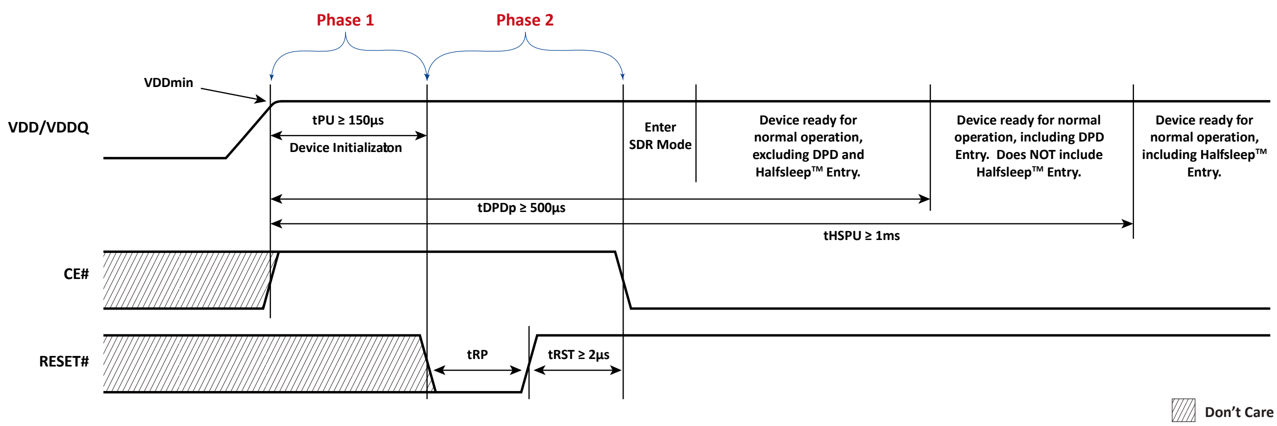


Figure 1. Power-Up Initialization Method 1 RESET#

The RESET# pin can also be used at any time after the device is initialized to reset all register contents. Memory content is not guaranteed. Timing requirements for RESET# usage are shown below.

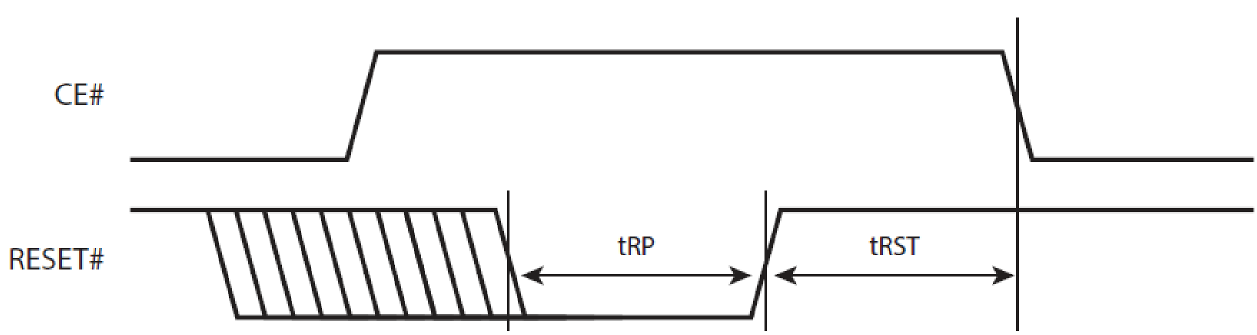


Figure 2. RESET# Timing

7.2 Power-Up Initialization Method 2 (via. Global Reset)

As an alternate power-up initialization method, After the Phase 1 150μs period the Global Reset command is used to reset the device in Phase 2 as follows:

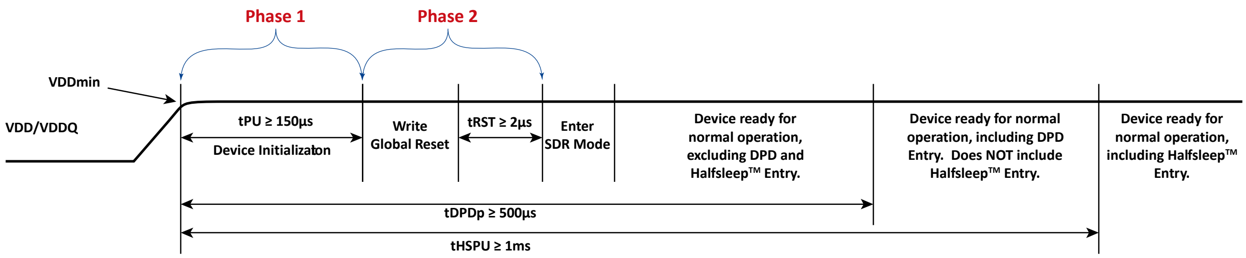


Figure 3. Power-Up Initialization Method 2 Timing with Global Reset

The Global Reset command resets all register contents. Memory content is not guaranteed. The command frame is made of 4 clocked CE# lows. Clocking is optional during tRST. The Global Reset command sequence is shown below. Note that Global Reset command can be used ONLY as Power-up initialization.

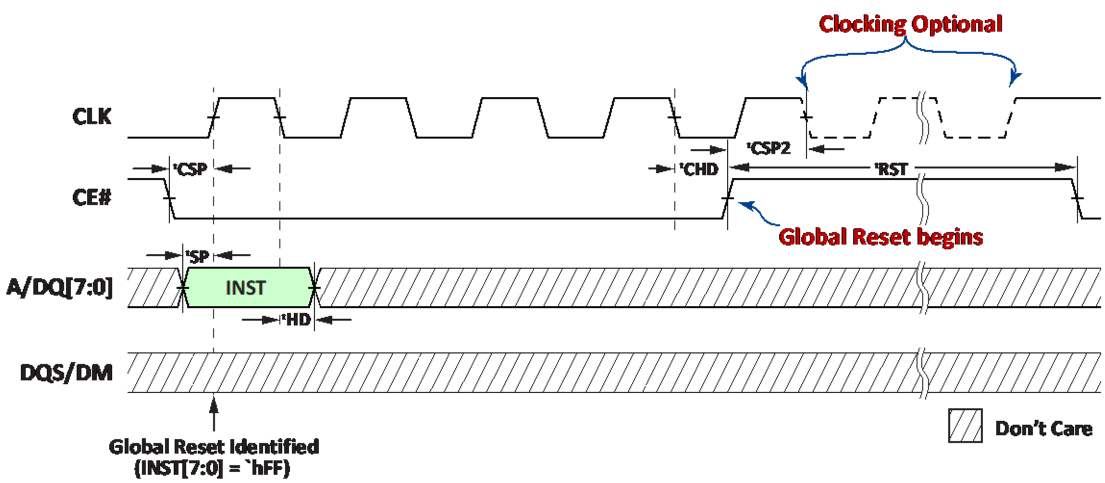


Figure 4: Global Reset

8 Interface Description

8.1 Address Space

Octal DDR PSRAM device is byte-addressable. Memory accesses are required to start on even addresses (A[0]='0). Mode Register accesses allow both even and odd addresses.

8.2 Burst Type & Length

Read and write operations are default Hybrid Wrap 32 mode. Other burst lengths of 16, 32, 64 or 1K bytes in standard or Hybrid wrap modes are register configurable(see Table 20). The device also includes command for Linear Bursting. Bursts can start on any even address. Write burst length has a minimum of 2 bytes. Read has no minimum length. Both write and read have no restriction on maximum burst length as long as tCEM is met.

8.3 Command/Address Latching

After CE# goes LOW, instruction code is latched on 1st CLK rising edge. Access address is latched on the 3rd, 4th, 5th & 6th CLK edges (2nd CLK rising edge, 2nd CLK falling edge, 3rd CLK rising edge, 3rd CLK falling edge).

8.4 Command Truth Table

The Octal DDR PSRAM recognizes the following commands specified on the INST (Instruction) cycle defined by the Address/DQ pins.

Note that Linear Burst commands, 20h and A0h, ignore burst setting defined by MR8[2:0].
Note that only Linear Burst Read command is capable of performing row boundary crossing (RBX) read function.

	1st CLK		2nd CLK		3rd CLK	
Command	↑	↓	↑	↓	↑	↓
Sync Read	00h		A3	A2	A1	A0
Sync Write	80h		A3	A2	A1	A0
Sync Read (Linear Burst)	20h		A3	A2	A1	A0
Sync Write (Linear Burst)	A0h		A3	A2	A1	A0
Mode Register Read	40h		×			MA
Mode Register Write	C0h		×			MA
Global Reset	FFh		×			

Remarks:
× = don't care (V_{IH}/V_{IL})
A3 = unused address bits are reserved
A2 = 1'bx, RA[12:6], unused address bit is reserved
A1 = RA[5:0],CA[9:8]
A0 = CA[7:0]
MA = Mode Register Address

8.5 Read Operation

After address latching, the device initializes DQS/DM to '0 from **next** CLK rising edge of the 3rd clock cycle (A1). See Figure 5 below.

Output data is available after LC latency cycles, as shown in Figure 7 & Figure 8, LC is defined in Table 5 and Table 6. When data is valid, A/DQ[7:0] and DQS/DM follow the timing specified in Figure 9. Synchronous timing parameters are shown in Table 30 & Table 31.

In case of internal refresh insertion, variable latency output data may be delayed by up to (LC*2) latency cycles as shown in Figure 7. True variable refresh pushout latency can be anywhere **between** LC to LCx2. The 1st DQS/DM rising edge after read pre-amble indicates the beginning of valid data.

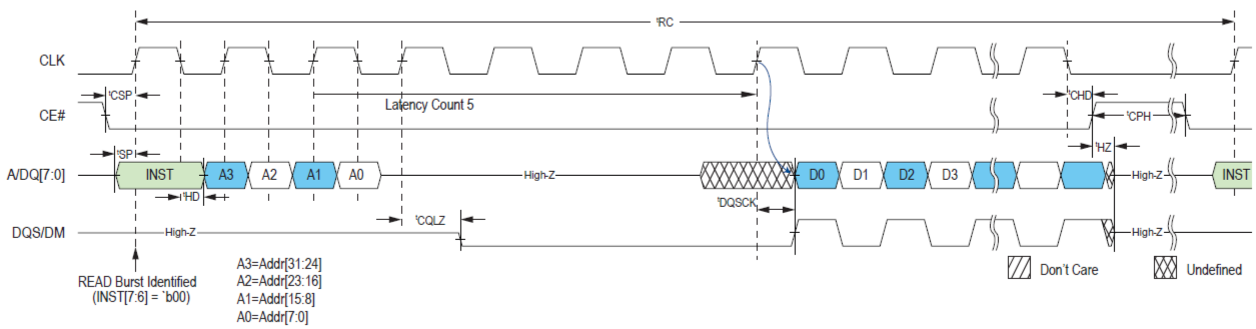


Figure 5: Synchronous Read

If RBX has been enabled (MR8[3] written to 1) and a Linear Burst Command issued, then Wrap settings (MR8[2:0] are ignored and Read operations are allowed to cross row boundaries as shown in Figure 6.

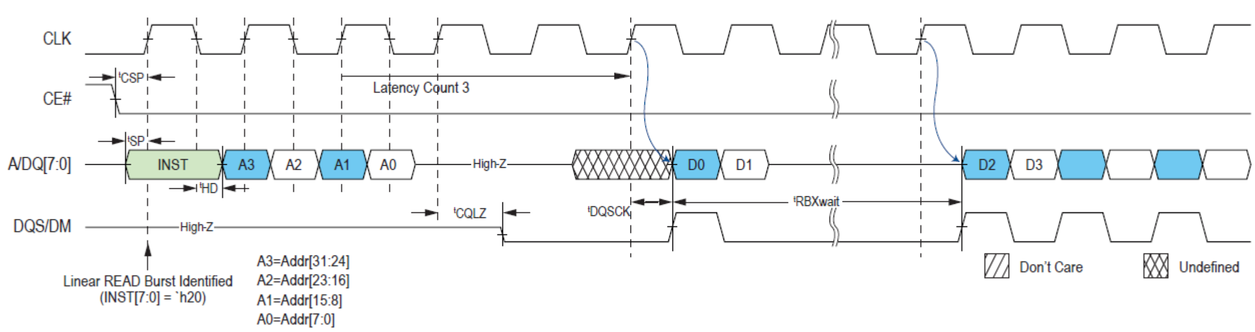


Figure 6: Synchronous Read with RBX (Starting address '3FE)

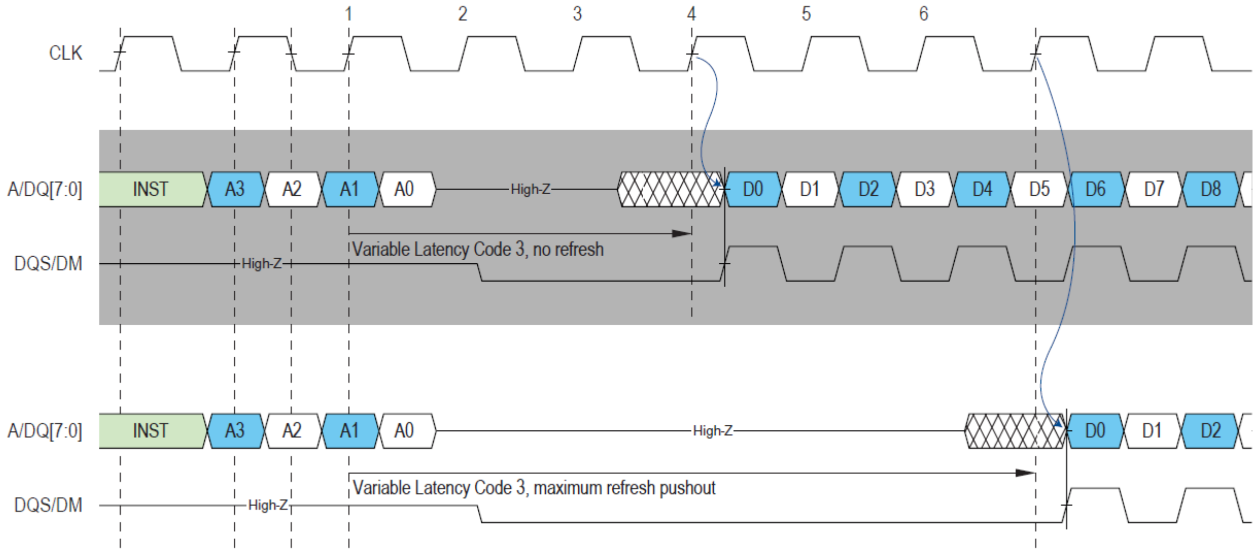


Figure 7: Variable Read Latency Refresh Pushout

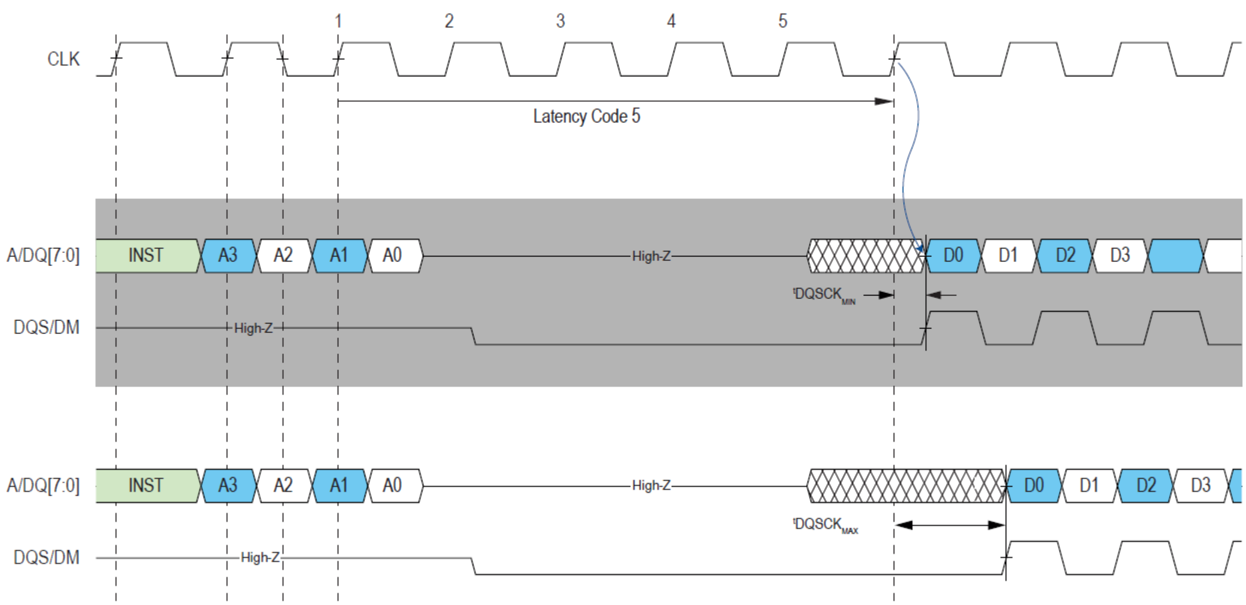


Figure 8: Read Latency & tDQSCK

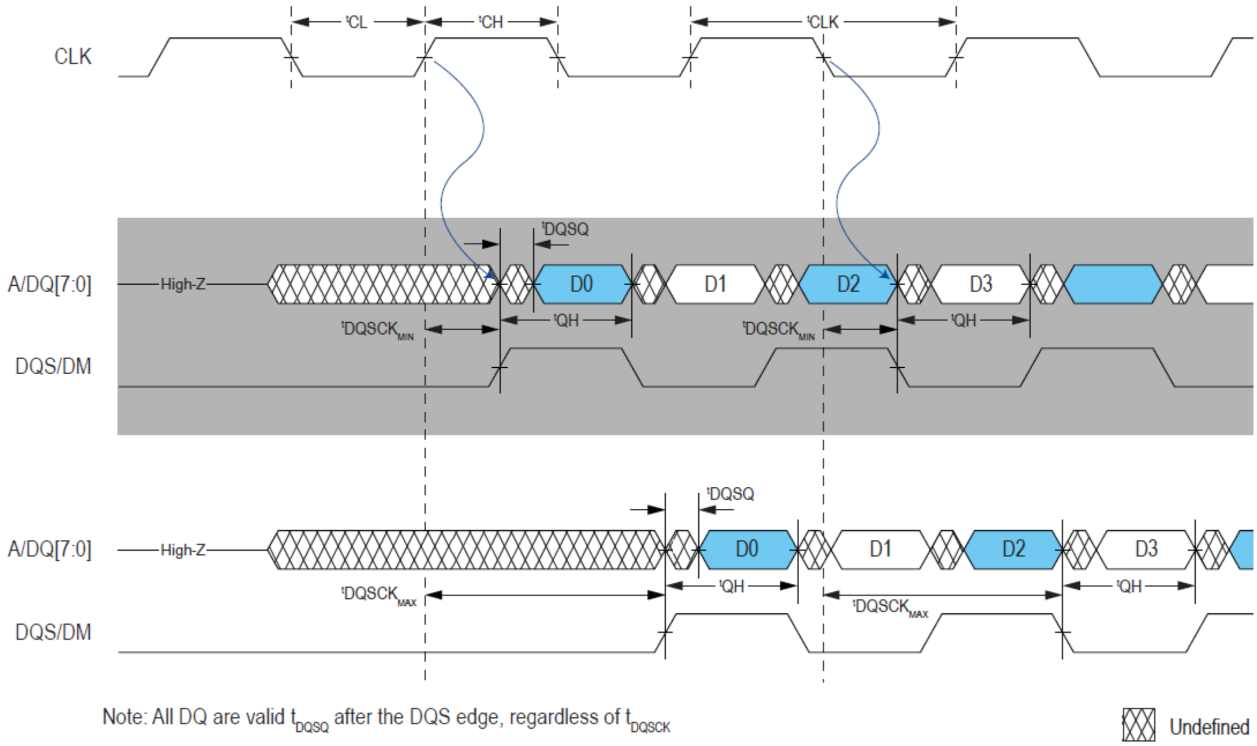


Figure 9: Read DQS/DM & DQ timing

8.6 Write Operation

A minimum of 2 bytes of data must be input in a write operation. In the case of consecutive short burst writes, tRC must be met by issuing additional CE# high time between operations. Single-byte write operations can be performed by masking the un-written byte with DQS/DM as shown in Figure 10.

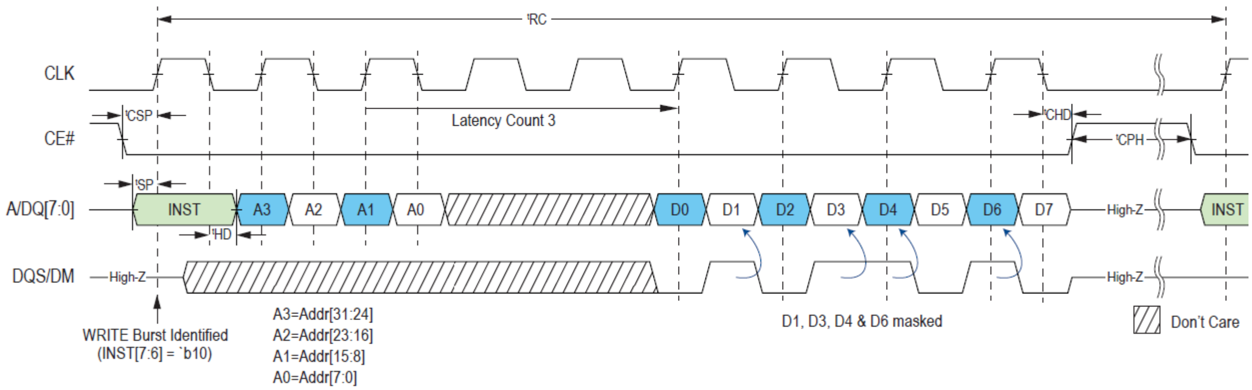


Figure 10: Synchronous Write followed by any Operation

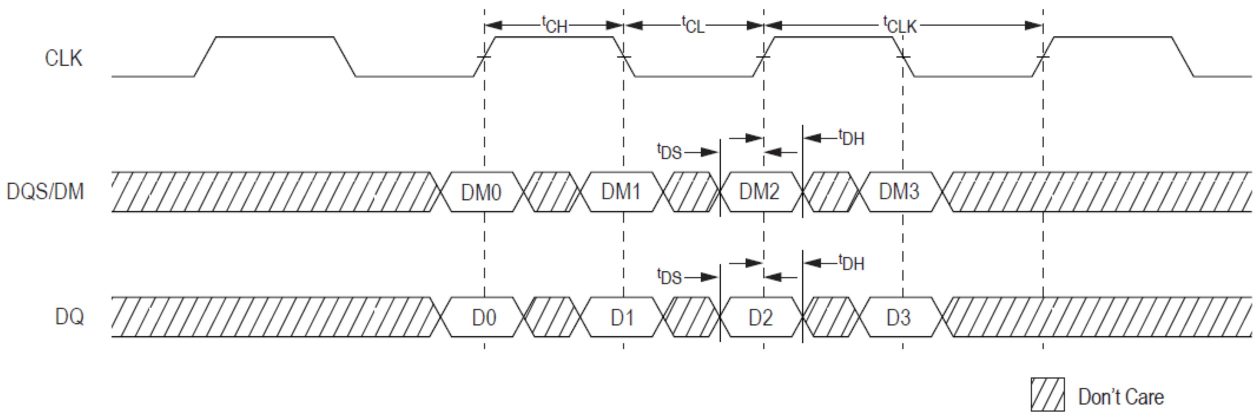
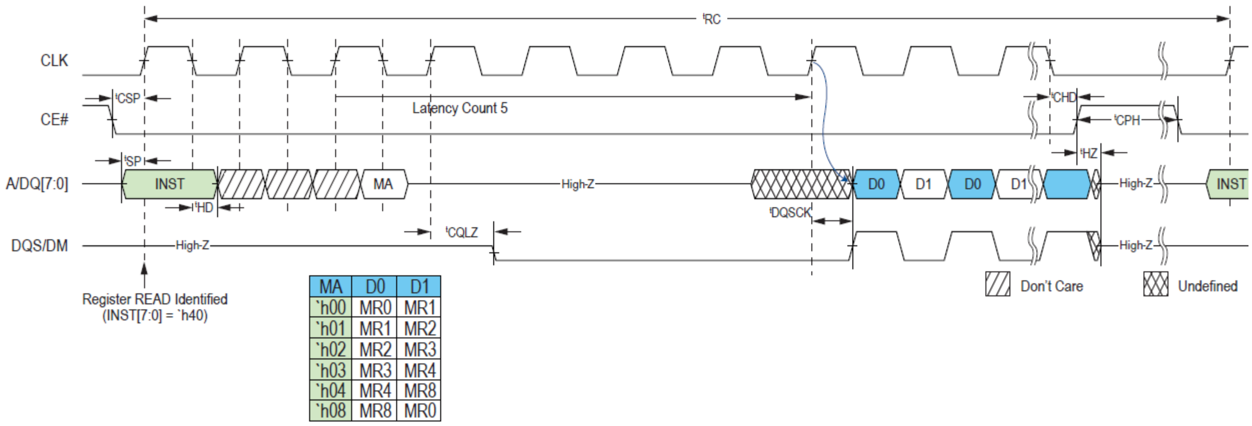


Figure 11: Write DQS/DM & DQ Timing

8.7 Control Registers

Register Read is shown below. Mode Address in command determines which Mode Register is read from as Data0 (see chart in the Figure below).



MA	D0	D1
`h00	MR0	MR1
`h01	MR1	MR2
`h02	MR2	MR3
`h03	MR3	MR4
`h04	MR4	MR8
`h08	MR8	MR0

Figure 12: Register Read

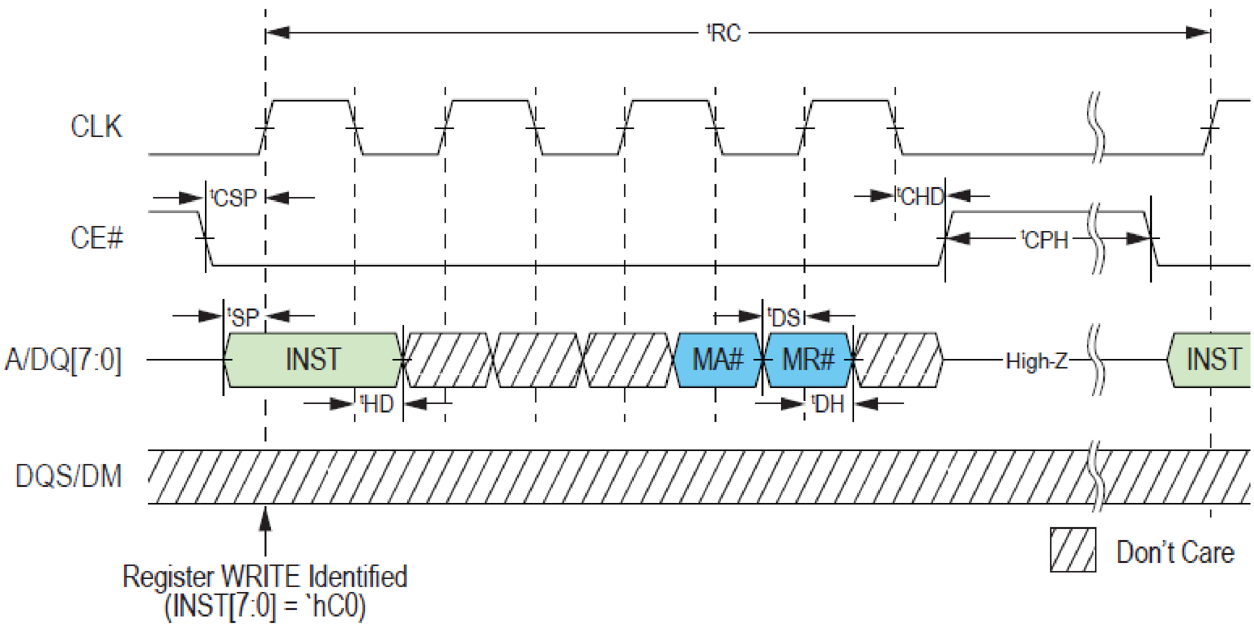


Figure 13: Register Write

Register Writes are Latency 1, whereas Register Reads use the same MR0[4:2] settings as burst reads (see Table 5). Registers 0, 4 & 8 are read and writable, and Registers 1, 2 and 3 are read-only. Register mapping is shown in Table 3. Note that MR0[6], MR0[7], MR4[4] and MR8[7] must be written to b'0.

Table 3: Mode Register Table

MR No.	MA[7:0]	Access	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
0	`h00	R/W	'00'		LT	Read Latency Code			Drive Str.	
1	`h01	R	ULP	rsvd.		Vendor ID				
2	`h02	R	GB	rsvd.		Dev ID		Density		
3	`h03	R	RBXen	VCC	SRF	rsvd.				
4	`h04	R/W	Write Latency Code			'0'	RF	PASR		
6	`h06	W	Halfsleep™ & DPD				rsvd.			
8	`h08	R/W	'0'	rsvd.			RBX	BT	BL	

Table 4: Read Latency Type (MR0[5])

Latency Type	
MR0[5]	LT
0	Variable (default)
1	Fixed

Table 5: Read Latency Codes MR0[5:2]

	VL Codes (MR0[5]=0)		FL Codes (MR0[5]=1)	Max Input CLK Freq (MHz)	
MR0[4:2]	Latency (LC)	Max push out (LCx2)	Latency (LCx2)	Standard	Extended
000	3	6	6	66	66
001	4	8	8	109	109
010	5 (default)	10	10	133	133
011	6	12	12	166	166
100	7	14	14	200	200
others	reserved			-	-

Table 6: Operation Latency Code Table

Type	Operation	VL (default)		FL
		No Refresh	Refresh	
Memory	Read	LC	Up to LCx2	LCx2
	Write	WLC		WLC
Register	Read	LC		LC
	Write	1		1

*Note: see Table 16 for WLC settings.

Table 7: Drive Strength Codes MR0[1:0]

Codes	*Drive Strength*
‘00	Full (25Ω)
‘01	Half (50Ω default)
‘10	1/4 (100Ω)
‘11	1/8 (200Ω)

Table 8: Ultra Low Power Device mapping MR1[7]

ULP	
‘0	Non-ULP (no Halfsleep™)
‘1	ULP (Halfsleep™ supported)

Table 9: Vendor ID mapping MR1[4:0]

Vendor ID
01101: APM

Table 10: Good-Die Bit MR2[7]*

Codes	*Good Die ID*
‘1	PASS
‘0	FAIL

*Note: Default is FAIL die, and only mark PASS after all tests passed.

Table 11: Device ID MR2[4:3]

Codes	*Device ID*
‘00	Generation 1
‘01	Generation 2
‘10	Generation 3 (default)
others	reserved

Table 12: Device Density mapping MR2[2:0]

MR2[2:0]	Density
‘001	32Mb
‘011	64Mb (default)
‘101	128Mb
‘111	256Mb
‘110	512Mb
others	reserved

Table 13: Row Boundary Crossing Enable (MR3[7])

MR3[7] (read-only)	*RBXen*
0	RBX not supported
1	RBX supported via MR8[3]=1

Table 14: Operating Voltage Range (MR3[6])

MR3[6]	*VCC*
0	1.8V (default)
1	3V

Table 15: Self Refresh Flag (MR3[5])

MR3[5] (read-only)	*Self Refresh Flag*
0	Slow Refresh (allowed via MR4[3]=1, otherwise Fast Refresh)
1	Fast Refresh

MR3[5] is a refresh indicator that corresponds to device internal temperature. This bit will indicate 0 when the temperature is low enough to allow a slow frequency refresh rate.

Table 16: Write Latency MR4[7:5]

Default powered up behavior is WL 5

MR4[7:5]	*Write Latency*	*Fmax (MHz)*
000	3	66
100	4	104
010	5 (default)	133
110	6	166
001	7	200
others	reserved	-

Table 17: Refresh Frequency MR4[3]

MR4[3]	*Refresh Frequency*
0	Fast Refresh (default)
1	Enables Slow Refresh when temperature allows

Table 18: PASR MR4[2:0]

The PASR bits restrict refresh operation to a portion of the total memory array. This feature allows the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map.

64Mb				
Codes	***Refresh Coverage***	***Address Space***	***Size***	***Density***
‘000	Full array (default)	000000h-7FFFFFh	8M x8	64Mb
‘001	Bottom 1/2 array	000000h-3FFFFFh	4M x8	32Mb
‘010	Bottom 1/4 array	000000h-1FFFFFh	2M x8	16Mb
‘011	Bottom 1/8 array	000000h-0FFFFFh	1M x8	8Mb
‘100	None	0	0M	0Mb
‘101	Top 1/2 array	400000h-7FFFFFh	4M x8	32Mb
‘110	Top 1/4 array	600000h-7FFFFFh	2M x8	16Mb
‘111	Top 1/8 array	700000h-7FFFFFh	1M x8	8Mb

Table 19: ULP Modes MR6[7:0]

MR6[7:0]	ULP Modes
'hF0	Halfsleep™
'hC0	Deep Power Down
others	reserved

Note: see 8.8 **HalfsleepTM** Mode; 8.9 Deep Power Down Mode for more information.

Table 20: Burst Type MR8[2], Burst Length MR8[1:0]

By default the device powers up in 32 Byte Hybrid Wrap. In non-Hybrid burst (MR8[2]=0), MR8[1:0] sets the burst address space in which the device will continually wrap within. If Hybrid burst wrap is selected (MR8[2]=1), the device will burst through the initial wrapped burst length once, then continue to burst incrementally up to maximum column address (1K) before wrapping around within the entire column address space. Burst length (MR8[1:0]) can be set to 16,32,64 & 1K lengths.

MR8[2]	MR8[1:0]	Burst Length	Example of Sequence of Bytes During Wrap	
			Starting Address	Byte Sequence
'0	'00	16 Byte Wrap	4	[4,5,6,...15,0,1,2,...]
'0	'01	32 Byte Wrap	4	[4,5,6,...31,0,1,2,...]
'0	'10	64 Byte Wrap	4	[4,5,6,...63,0,1,2,...]
'0	'11	1K Byte Wrap	4	[4,5,6,...1023,0,1,2,...]
'1	'00	16 Byte Hybrid Wrap	2	[2,3,4,...15,0,1],16,17,18,...1023,0,1,...
'1	'01	32 Byte Hybrid Wrap (default)	2	[2,3,4,...31,0,1],32,33,34,...1023,0,1,...
'1	'10	64 Byte Hybrid Wrap	2	[2,3,4,...63,0,1],64,65,66,...1023,0,1,...
'1	'11	1K Byte Wrap	2	[2,3,4,...1023,0,1,2,...]

The Linear Burst Commands (INST[5:0]=6'b100000) override MR8[2:0] settings and forces the current array read or write command to do 1K Byte Wrap (equivalent to having MR8[1:0] set to 2'b11). The burst continues linearly from the starting address and at the end of the page, then wraps back to the beginning of the page. This special burst instruction can be used on both array write and read.

Table 21: Row Boundary Crossing Read Enable MR8[3]

This register setting applies to Linear Burst reads only on RBX enabled devices (MR3[7]=1). Default write and read burst behavior is limited within the 1K (CA='h000 -> 'h3FF) column address space. Setting this bit high will allow Linear Burst reads to cross over into the next Row (RA+1).

MR8[3]	RBX Read
0	Reads stay within the 1K column address space
1	Reads cross row at 1K boundaries

8.8 Halfsleep™ Mode

Halfsleep™ Mode is a feature which puts the device in an ultra-low power state, while the stored data is retained. Halfsleep™ Mode Entry is entered by writing 8'hF0 into MR6. CE# going high initiates the Halfsleep™ mode and must be maintained for the minimum duration of tHS. The Halfsleep™ Entry command sequence is shown below.

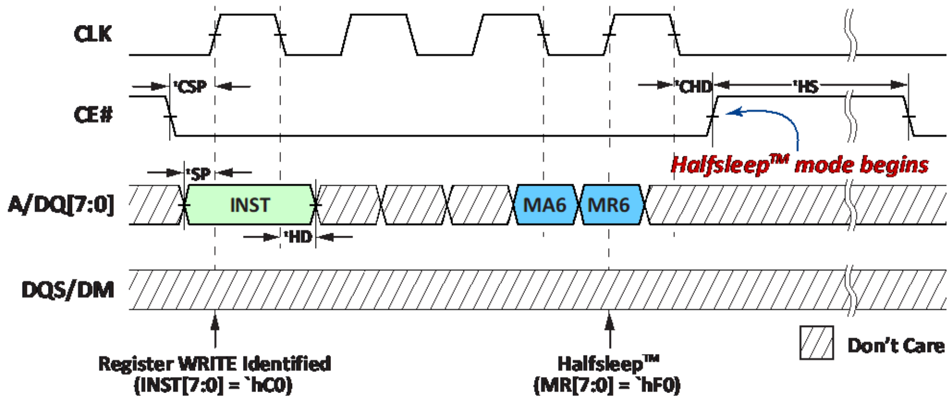


Figure 14: Halfsleep™ Entry Write (default WL0)

Halfsleep™ Exit is initiated by a low pulsed CE#. Afterwards, CE# can be held high with or without clock toggling until the first operation begins (observing minimum tXHS).

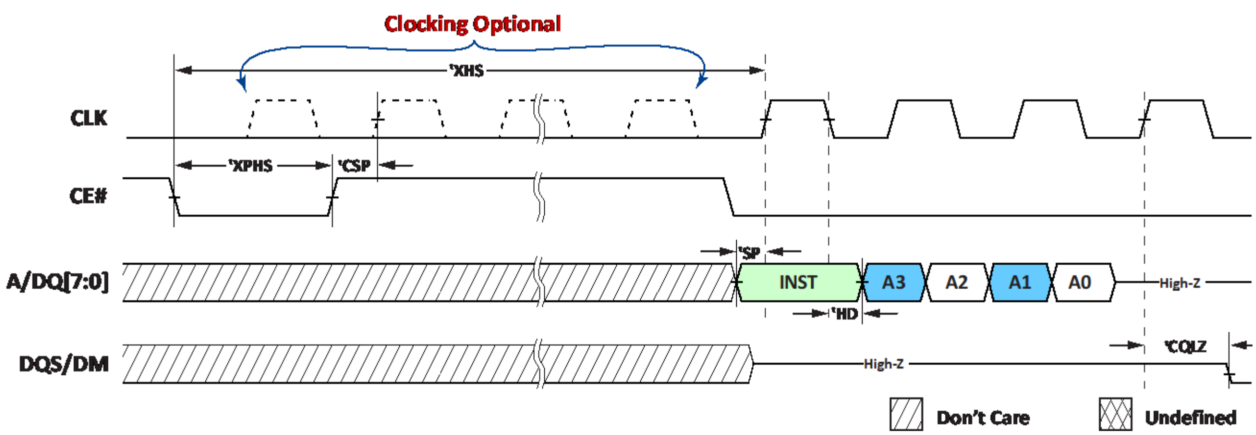


Figure 15: Halfsleep™ Exit (Read Operation shown as example)

8.9 Deep Power Down Mode

Deep Power Down Mode (DPD) is a feature which puts the device into power down state. DPD Mode Entry is entered by writing 8'hC0 into MR6. CE# going high initiates the DPD Mode and must be maintained for the minimum duration of tDPD. The Deep Power Down Entry command sequence is shown below.

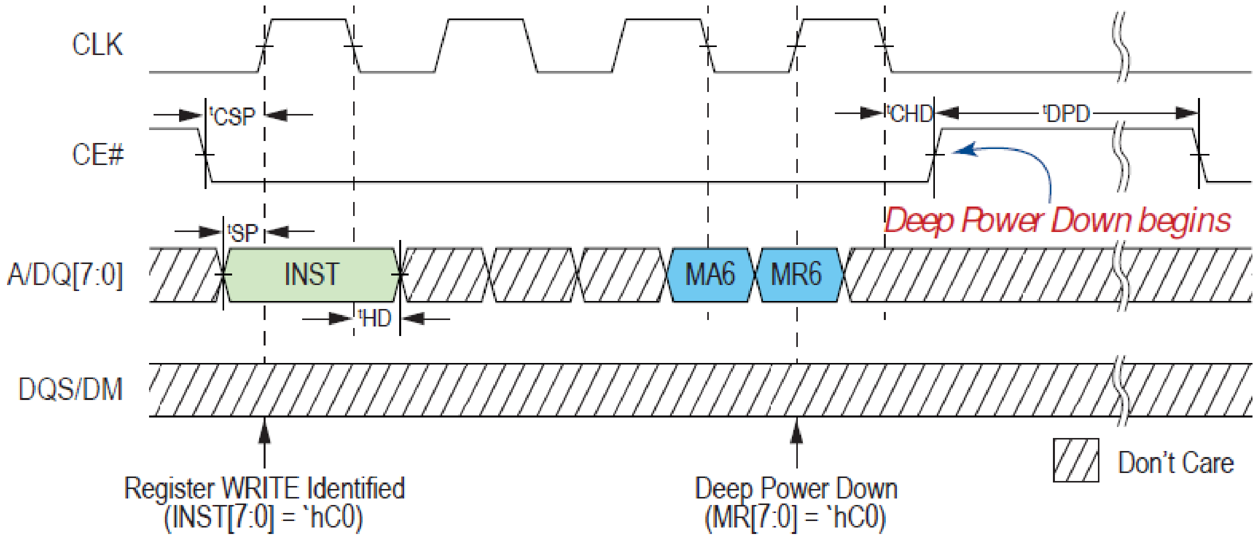


Figure 16: Deep Power Down Entry

Deep Power Down Exit is initiated by a low pulsed CE#. After a CE# DPD Exit, CE# must be held high with or without clock toggling until the first operation begins (observing minimum tXDPD).

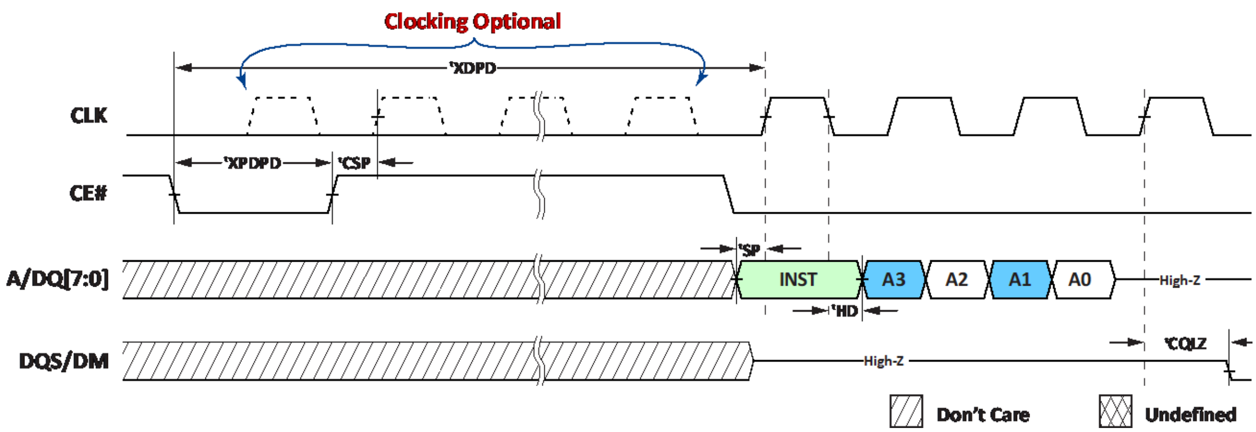


Figure 17: Deep Power Down Exit (Read Operation shown as example)

Register values and memory content are not retained in DPD Mode. After DPD mode register values will reset to defaults. tDPDp is minimum period between two DPD Modes (measured from DPD exit to the next DPD entry) as well as from the initial powerup to the first DPD entry.

9 Electrical Specifications:

9.1 Absolute Maximum Ratings

Table 22: Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Voltage to any ball except V_{DD}, V_{DDQ} relative to V_{SS}	VT	-0.4 to V_{DD}/V_{DDQ}+0.4	V	
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	-0.4 to +2.45	V	
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	-0.4 to +2.45	V	
Storage Temperature	T_{STG}	-55 to +150	°C	1

Notes 1: Storage temperature refers to the case surface temperature on the center/top side of the PSRAM.

Caution:
Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

9.2 Pin Capacitance

Table 23: Bare Die Pin Capacitance

Parameter	Symbol	Min	Max	Unit	Notes
Input Pin Capacitance	CIN		2	pF	VIN=0V
Output Pin Capacitance	COUT		3	pF	VOUT=0V

Note: spec'd at 25°C.

Table 24: Package Pin Capacitance

Parameter	Symbol	Min	Max	Unit	Notes
Input Pin Capacitance	CIN		6	pF	VIN=0V
Output Pin Capacitance	COUT		8	pF	VOUT=0V

Note: spec'd at 25°C.

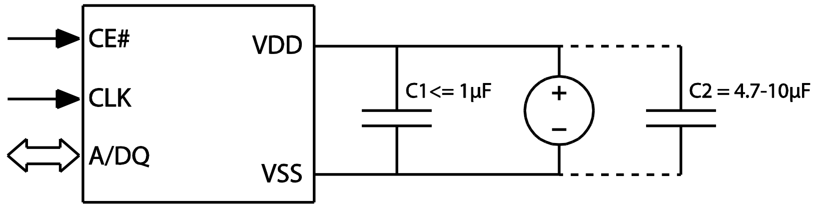
Table 25: Load Capacitance

Parameter	Symbol	Min	Max	Unit	Notes
Load Capacitance	C_L		15	pF	

Note: System C_L for the use of package

9.3 Decoupling Capacitor Requirement

System designers need to take care of power integrity considering voltage regulator response and the memory peak currents/usage modes.



9.3.1 Low ESR cap C1:

It is recommended to place a low ESR decoupling capacitor of <=1µF close to the device to absorb transient peaks.

9.3.2 Large cap C2:

During Halfsleep™ modes even though Halfsleep™ average currents are very small (less than 100µA), device will internally have low duty cycle burst refresh for an extended period of time of a few tens of microseconds. These refresh current peaks are large. During this period if the system regulator cannot supply large peaks for several microseconds, it is important to place a 4.7µF-10µF cap to take care of burst refresh currents and replenish the charge before next burst of refreshes.

If required please contact AP Memory for further current peak details.

9.4 Operating Conditions

Table 26: Operating Characteristics

Parameter	Min	Max	Unit	Notes
Operating Temperature (extended)	-40	105	°C	
Operating Temperature (standard)	-40	85	°C	

9.5 DC Characteristics

Table 27: DC Characteristics

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	Supply Voltage	1.62	1.98	V	
V_{DDQ}	I/O Supply Voltage	1.62	1.98	V	
V_{IH}	Input high voltage	V_{DDQ}-0.4	V_{DDQ}+0.2	V	
V_{IL}	Input low voltage	-0.2	0.4	V	
V_{OH}	Output high voltage (I_{OH}=-0.2mA)	0.8 V_{DDQ}		V	
V_{OL}	Output low voltage (I_{OL}=+0.2mA)		0.2 V_{DDQ}	V	
I_{LI}	Input leakage current		1	µA	
I_{LO}	Output leakage current		1	µA	
ICC	Read/Write @13MHz		4	mA	2
	Read/Write @133MHz		16	mA	2
	Read/Write @166MHz		19	mA	2
	Read/Write @200MHz		22	mA	2
ISB_{EXT}	Standby current (105C)		300	µA	1,3
ISB_{STD}	Standby current (85C)		200	µA	3
ISB_{STDDPD}	Standby current (Deep Power Down -40°C to 85°C)		15	µA	8

Note 1: Spec'd up to 105°C.
Note 2: Current is only characterized.
Note 3: Without CLK toggling. ISB will be higher if CLK is toggling.
Note 4: Slow Refresh.
Note 5: Typical $ISB_{STDROOM}$ 66uA.
Note 6: Current is only guaranteed after 150ms into Halfsleep™ mode.
Note 7: Typical ISB_{STDHS} 20uA
Note 8: Typical mean ISB_{STDDPD} 7uA at 25°C

9.6 ISB Partial Array Refresh Current

Table 28: Typical PASR Current @ 25°C

Standby Current @ 25°C			
PASR	***ISB –typical mean***	***Unit***	***Notes***
Full	66	µA	1,2
1/2	65	µA	1,2
1/4	64	µA	1,2
1/8	60	µA	1,2
Halfsleep™ Current @ 25°C			
PASR	***I Halfsleep™ -typical mean***	***Unit***	***Notes***
Full	20	µA	1,2,3
1/2	14	µA	1,2,3
1/4	11	µA	1,2,3
1/8	10	µA	1,2,3

Table 29: Typical PASR Current @ 85°C

Standby Current @ 85°C			
PASR	***ISB –typical mean***	***Unit***	***Notes***
Full	190	µA	2
1/2	150	µA	2
1/4	125	µA	2
1/8	110	µA	2
Halfsleep™ Current @ 85°C			
PASR	***I Halfsleep™ -typical mean***	***Unit***	***Notes***
Full	120	µA	2,3
1/2	72	µA	2,3
1/4	48	µA	2,3
1/8	24	µA	2,3

Note 1: Slow Refresh current is only attainable by enabling Slow Refresh Frequency (see Table 17)

Note 2: PASR Current is only characterized based on 64M density without CLK toggling.

Note 3: Spec'd Halfsleep™ current is only guaranteed after 150ms into Halfsleep™ mode.

9.7 AC Characteristics

Table 30: READ/WRITE Timing

		KGD/BGA 1.8V Only							
		-7(133MHz)		*-6(166MHz)*		*-5(200MHz)*			
Symbol	***Parameter***	***Min***	***Max***	***Min***	***Max***	***Min***	***Max***	***Unit***	***Notes***
tCLK	CLK period	7.5		6		5		ns	
tCH/tCL	Clock high/low width	0.45	0.55	0.45	0.55	0.45	0.55	tCLK	
tKHKL	CLK rise or fall time		1.2		1		0.8	ns	
tCPH	CE# HIGH between subsequent burst operations	15		18		20		ns	
tCEM	CE# low pulse width (excluding Halfsleep™ exit)		8		8		8	µs	Standard temp
			3		3		3	µs	Extended temp
tCEM	CE# low pulse width	3		3		3		tCLK	Minimum 3
tCSP	CE# setup time to CLK rising edge	2		2		2		ns	
tCSP2	CE# rising edge to next CLK falling edge	1.5		1.5		1.5		ns	
tCHD	CE# hold time from CLK falling edge	2		2		2		ns	
tSP	Setup time to active CLK edge	0.8		0.8		0.8		ns	
tHD	Hold time from active CLK edge	0.8		0.8		0.8		ns	Max 0.75*tCLK
tHZ	Chip disable to DQ/DQS output high-Z		6		6		6	ns	
tRBXwait	Row Boundary Crossing Wait Time	30	65	30	65	30	65	ns	
tRC	Write Cycle	60		60		60		ns	
tRC	Read Cycle	60		60		60		ns	
tHS	Minimum Halfsleep™ duration	150		150		150		µs	
tXHS	Halfsleep™ Exit CE# low to CLK setup time	150		150		150		µs	
tXPHS	Halfsleep™ Exit CE# low pulsewidth	60		60		60		ns	
			tCEM		tCEM		tCEM	µs	Standard temp
								µs	Extended temp
tDPD	Minimum DPD duration	500		500		500		µs	
tDPDp	Minimum period between DPD	500		500		500		µs	
tXDPD	DPD CE# low to CLK setup time	150		150		150		µs	
tXPDPD	DPD Exit CE# low pulsewidth	60		60		60		ns	
tPU	Device Initialization	150		150		150		µs	
tRP	RESET# low pulse width	1		1		1		µs	
tRST	Reset to CMD valid	2		2		2		µs	

Table 31: DDR timing parameters

Symbol	Parameter	KGD/BGA 1.8V Only -7(133MHz) Min	KGD/BGA 1.8V Only -7(133MHz) Max	-6(166MHz) Min	-6(166MHz) Max	-5(200MHz) Min	-5(200MHz) Max	Unit	Notes
tCQLZ	Clock rising edge to DQS low	1	6	1	6	1	6	ns	
tDQSCK	DQS output access time from CLK	2	5.5	2	5.5	2	5.5	ns	
tDQSQ	DQS – DQ skew		0.6		0.5		0.4	ns	
tDS	DQ and DM input setup time	0.8		0.8		0.8		ns	
tDH	DQ and DM input hold time	0.8		0.8		0.8		ns	

10 Change Log

Version	Who	Date	Description
1.0		Mar 02, 2017	Initial Version
1.1		Mar 03, 2017	Changed register usage for Refresh Frequency
1.2		Mar 27, 2017	Temperature range correction; reformatted PASR current
1.3		July 18, 2017	Tables, reworded burst table for clarity; added pin cap tables
1.4		Aug 01, 2017	Corrected tCQLZ reference edge
1.5		Aug 03, 2017	Corrected tCHD reference edge in table; add don't care data to Register Write drawing
1.6		Sep 11, 2017	Corrected extended temperature range; updated ordering information; added system CL for max frequency
1.7		Sep 25, 2017	Added Typical ISBSTDHS & note for latency count of register read
2.0		Oct 31, 2017	Removed Hybrid 64, modified Write 4 bytes & absolute voltage, VIL/VIH, added typical ISB & PASR@25C
2.1		Nov 13, 2017	Revised ICC and ISB
2.2		Nov 27, 2017	Revised typical ISB, HS ISB spec
2.3		Dec 21, 2017	Revised tCHD, WLC table
2.4		Jan 28, 2018	Restored timing of Half Sleep mode, corrected typo of Half Sleep mode
2.5		Apr 13, 2018	Added DPD
2.6		Apr 26, 2018	Revised cross-reference of Table 17 in table 27 and 28
2.7		Nov 30, 2018	Note for special part of OBM, updated some latency wording and added operation latency table
2.8		Jan 09, 2019	Unified part number to OBM for RBX read & special parts of STM32L4+ family
2.81		Jan 22, 2019	Updated Max. Frequency of ordering information
2.82		May 30, 2019	Added ISB_{STDDPD}, updated tXHS spec
2.83		May 31, 2019	Removed the NOTE for STM32L4+ family
2.9		Aug 06, 2019	Updated section 6 Power-Up Initialization; added table for change log; revised Page 1; revised section 4 table and picture; added notes for 24B BGA
3.0		Aug 08, 2019	Revised typo in Page 1; added b'0 notes for Table3; revised Table 11; corrected C_L in Table 25; Added tRBXwait in Table 30
3.1		Aug 16, 2019	Revised section 9.6, Table 15, Table 28 & Table 29; added section 9.3
3.1a		Aug 21, 2019	Updated notes of section 2 and Table 20; Updated Figure 1;
3.2		Sep 28, 2019	Updated header and page 1; updated ICC in Table 27; updated Table 28 and Table 29
3.3		Oct 30, 2019	Updated notes for Table 3, Table 15, Table 20 and section 8.5

3.4		Nov 14, 2019	Updated notes in section 8.5, Table 16, Table 18 and Table 30
3.4a		Nov 20, 2019	Updated typo in section 8.7
3.5a		Dec 11, 2019	Updated tHS_{min} in Table 30, Figure 15 and Figure 17
3.5b		Dec 13, 2019	Updated the notes for Table 27
3.6		Oct 18, 2021	tCEM revised data by BD suggest (E3_OPI_64Mb/128Mb) Standard temp: 4 us -> 8 us. Extended temp: 1 us -> 3 us.
3.6a		Dec 07, 2021	Revised some figure can't display grid (ex: Don't care/Undefined) when conversion to PDF.
3.7	Kim/ Eric/ Wayne	Aug 12,2022	Revised typos.